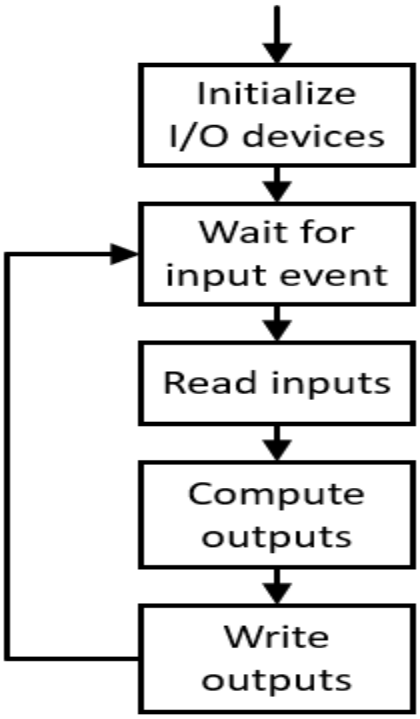
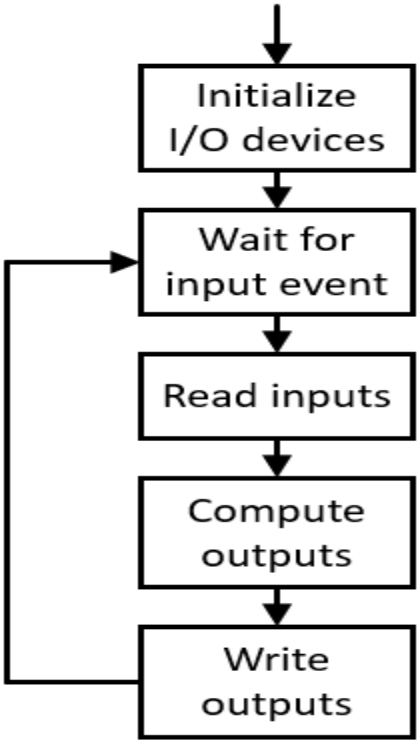
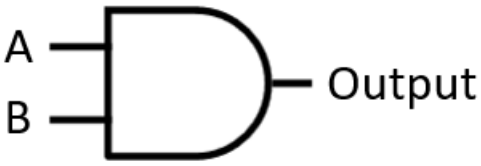
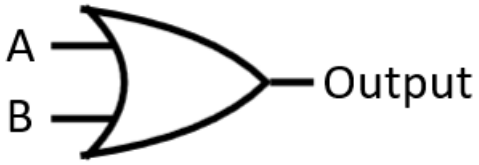
Chapter 1: Architecting High-Performance Embedded Systems.

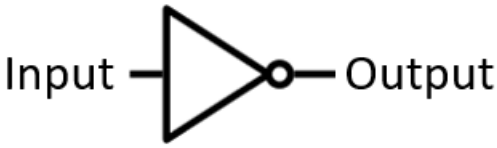


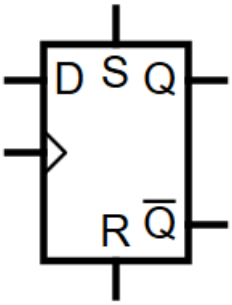


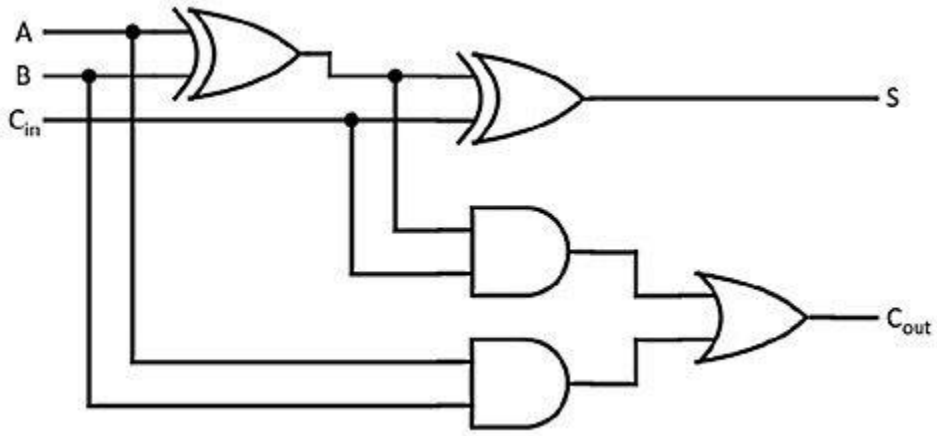

A
B
Output


A
B
Output

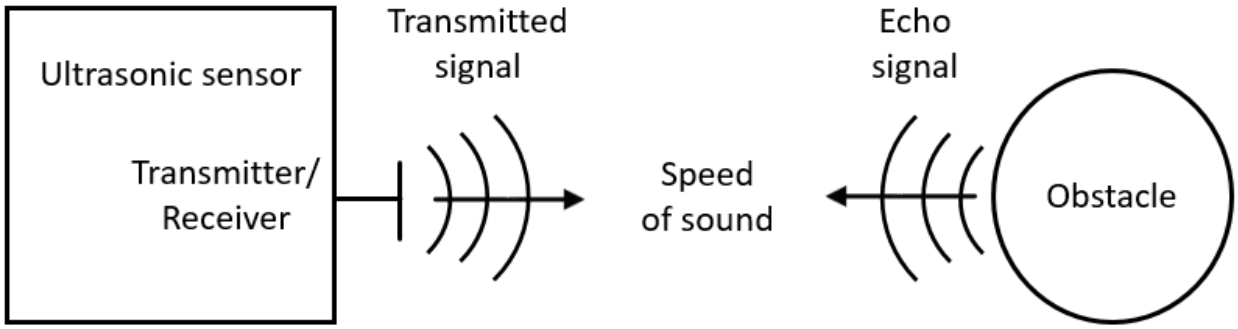

A
B
Output

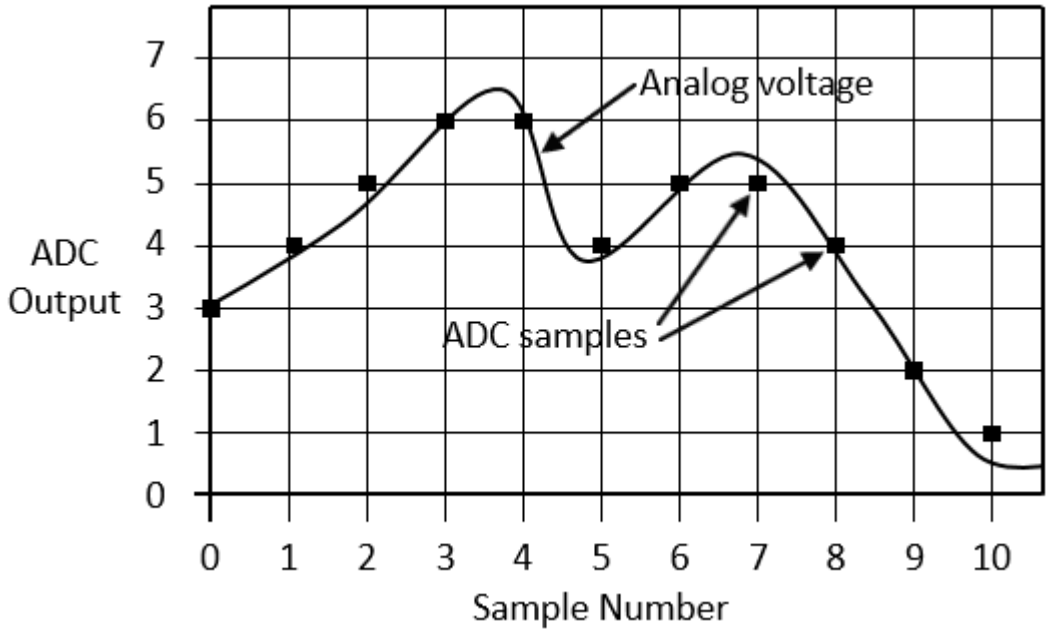

Input
Output

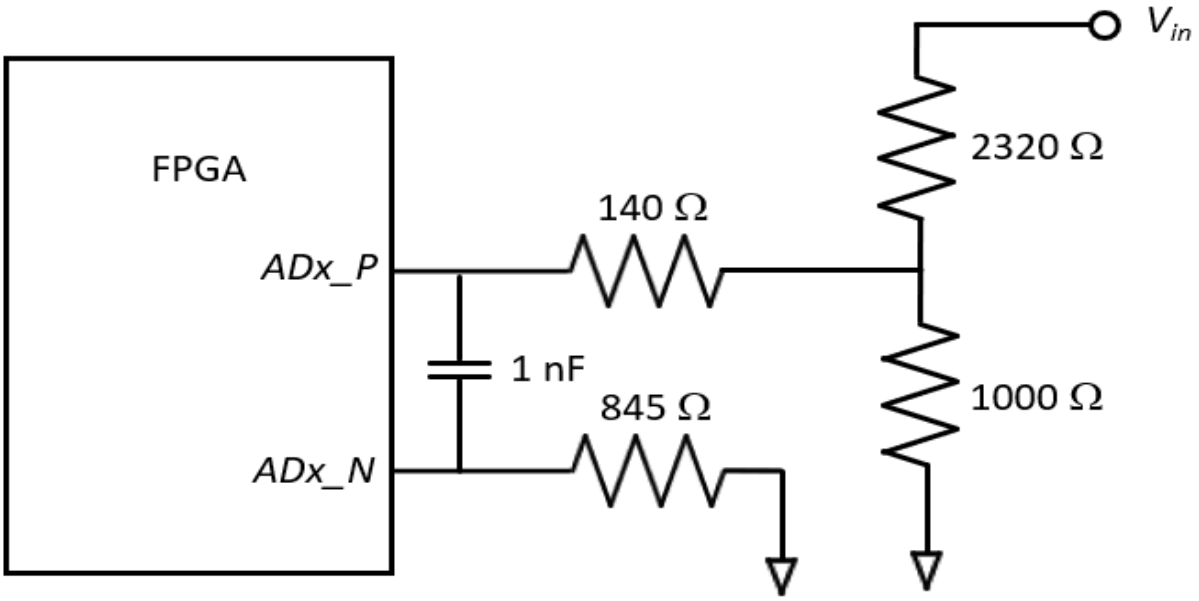

D
S
Q
R
$\overline{Q}$

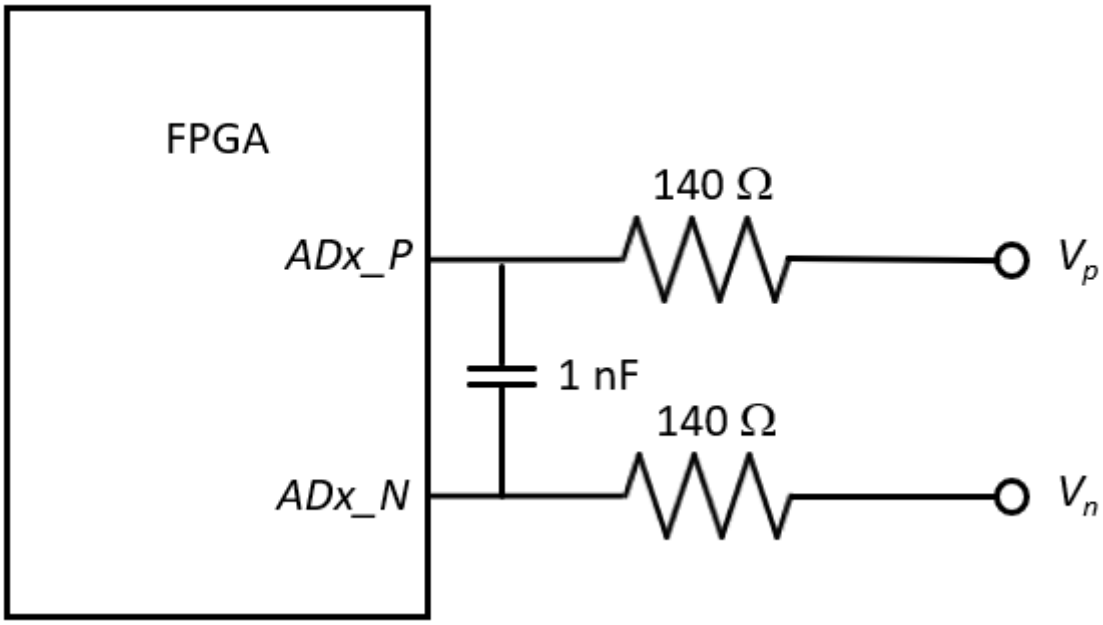

A
B
C_{in}
S
C_{out}

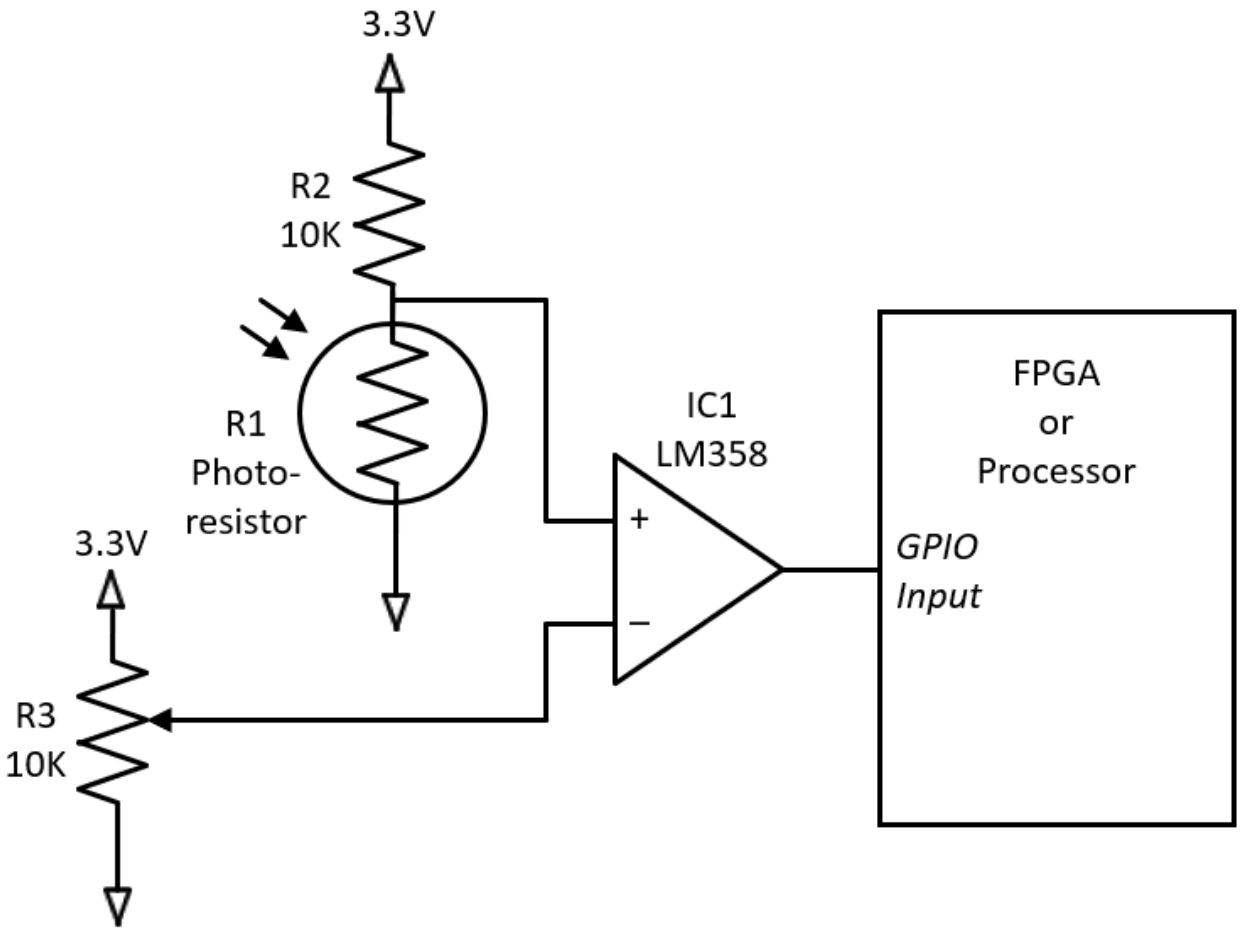
Chapter 2: Sensing the World

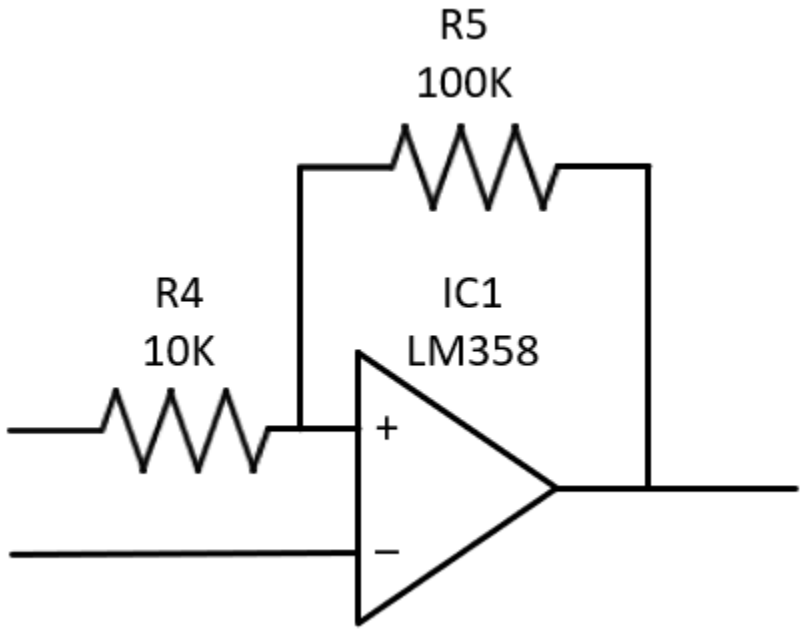


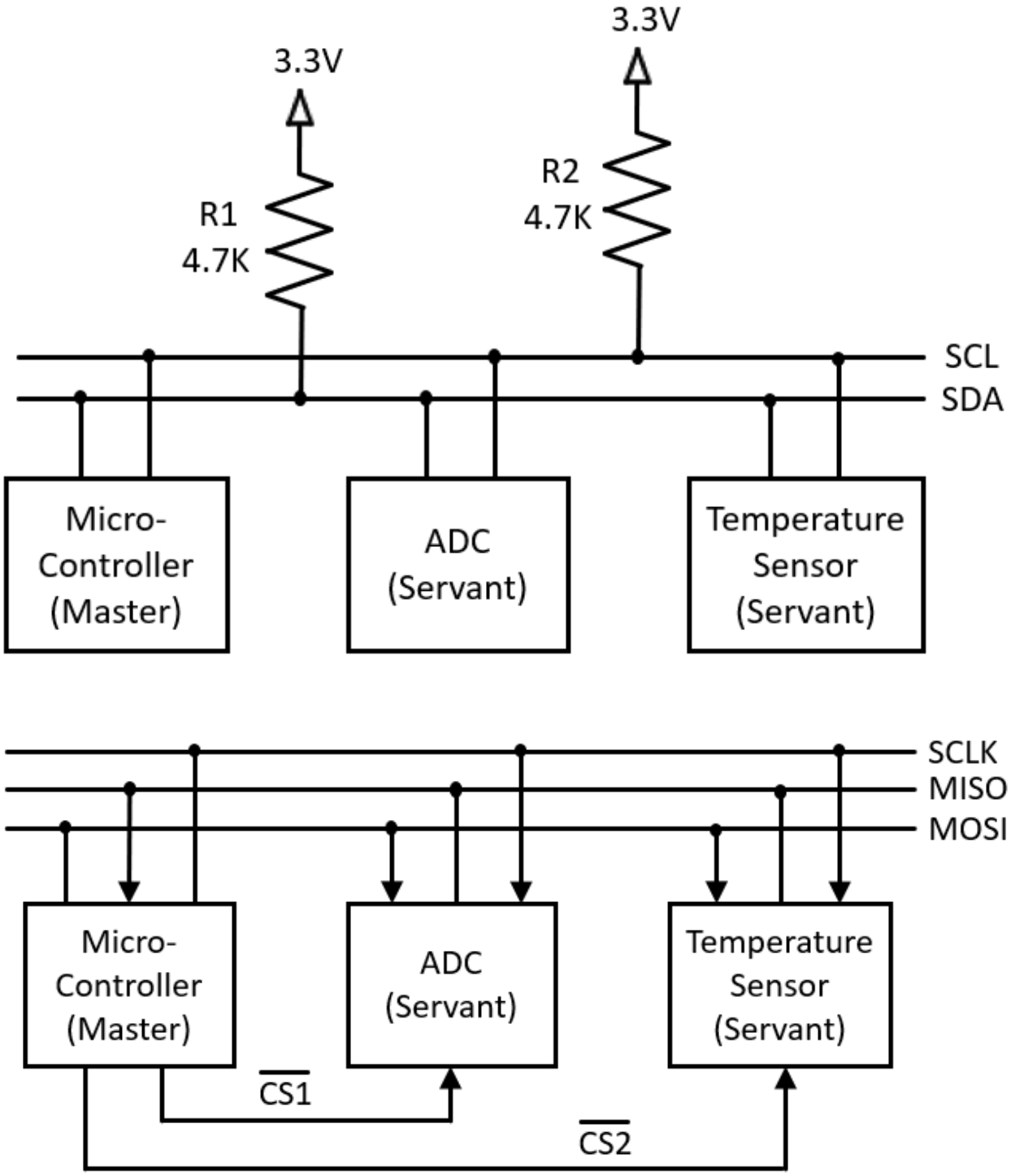


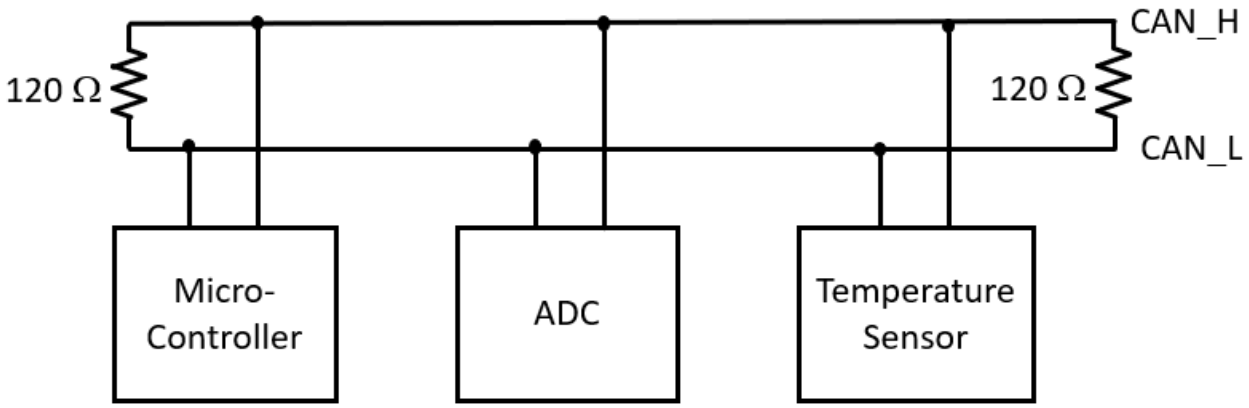

FPGA
ADx_P
ADx_N
140 Ω
1 nF
845 Ω
2320 Ω
1000 Ω
V_{in}


FPGA
ADx_P
ADx_N
140 Ω
1 nF
140 Ω
V_p
V_n

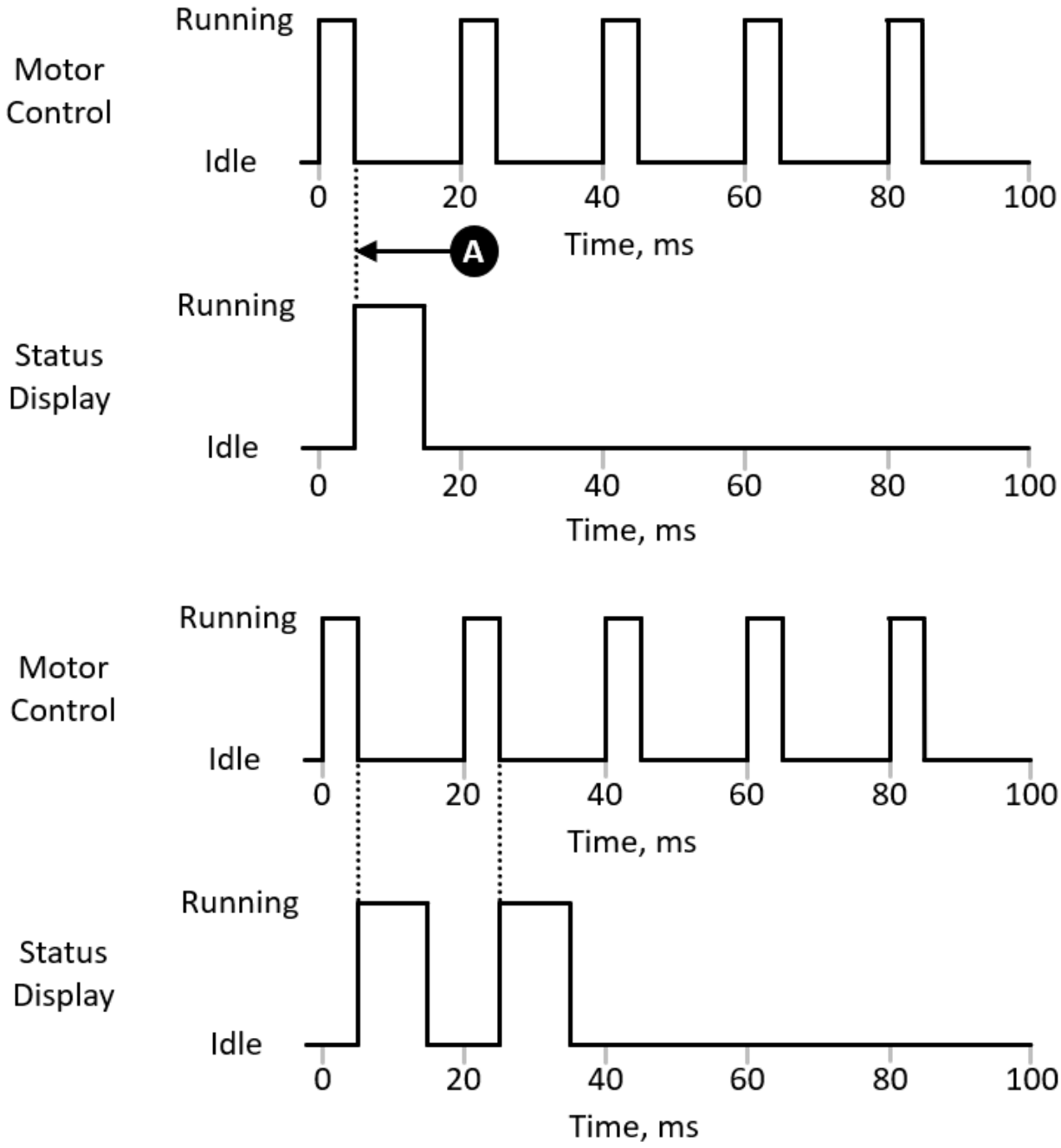

3.3V
R2
10K
R1
Photo-
resistor
IC1
LM358
FPGA
or
Processor
3.3V
GPIO
Input
R3
10K

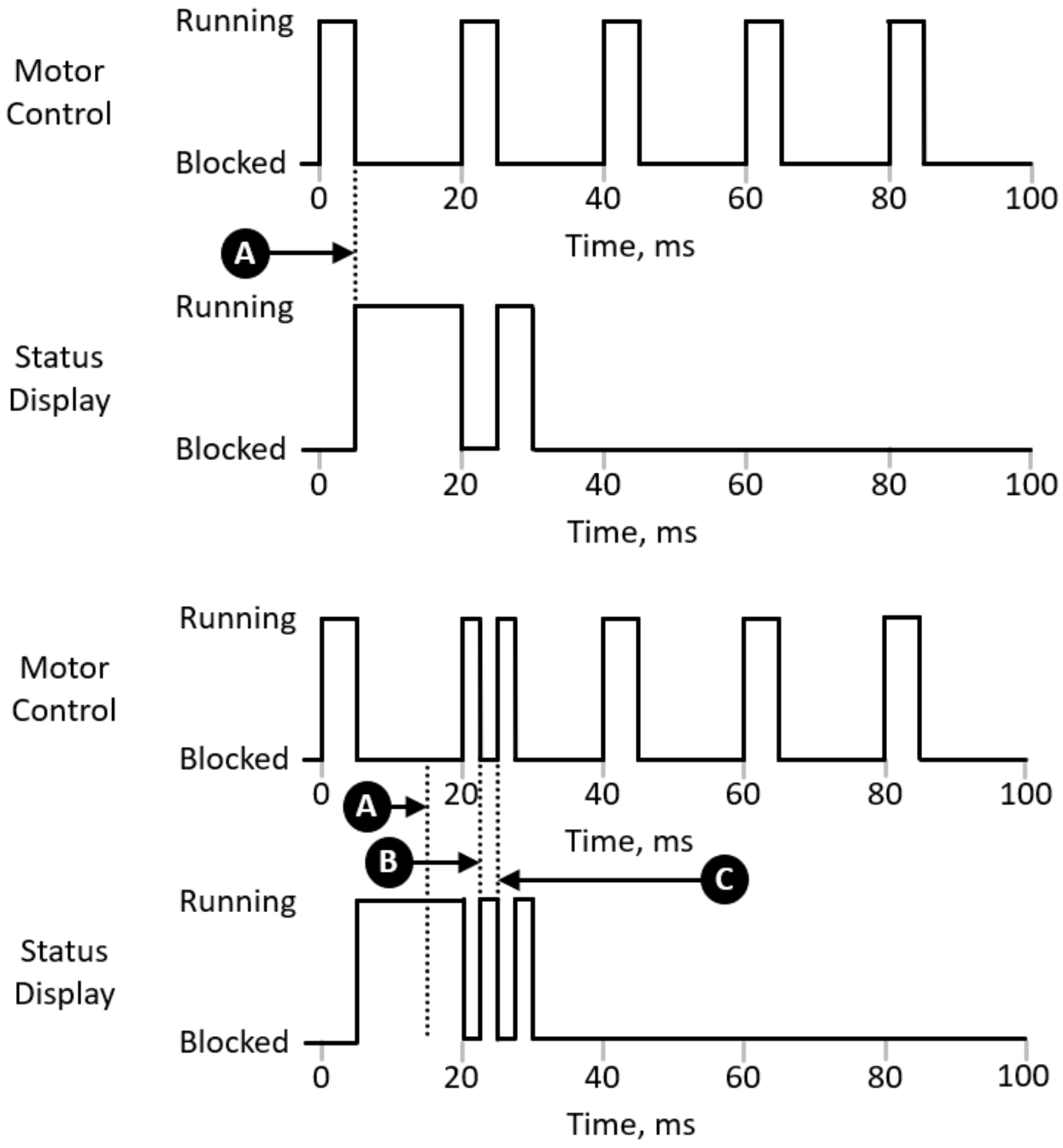

R5
100K
R4
10K
IC1
LM358

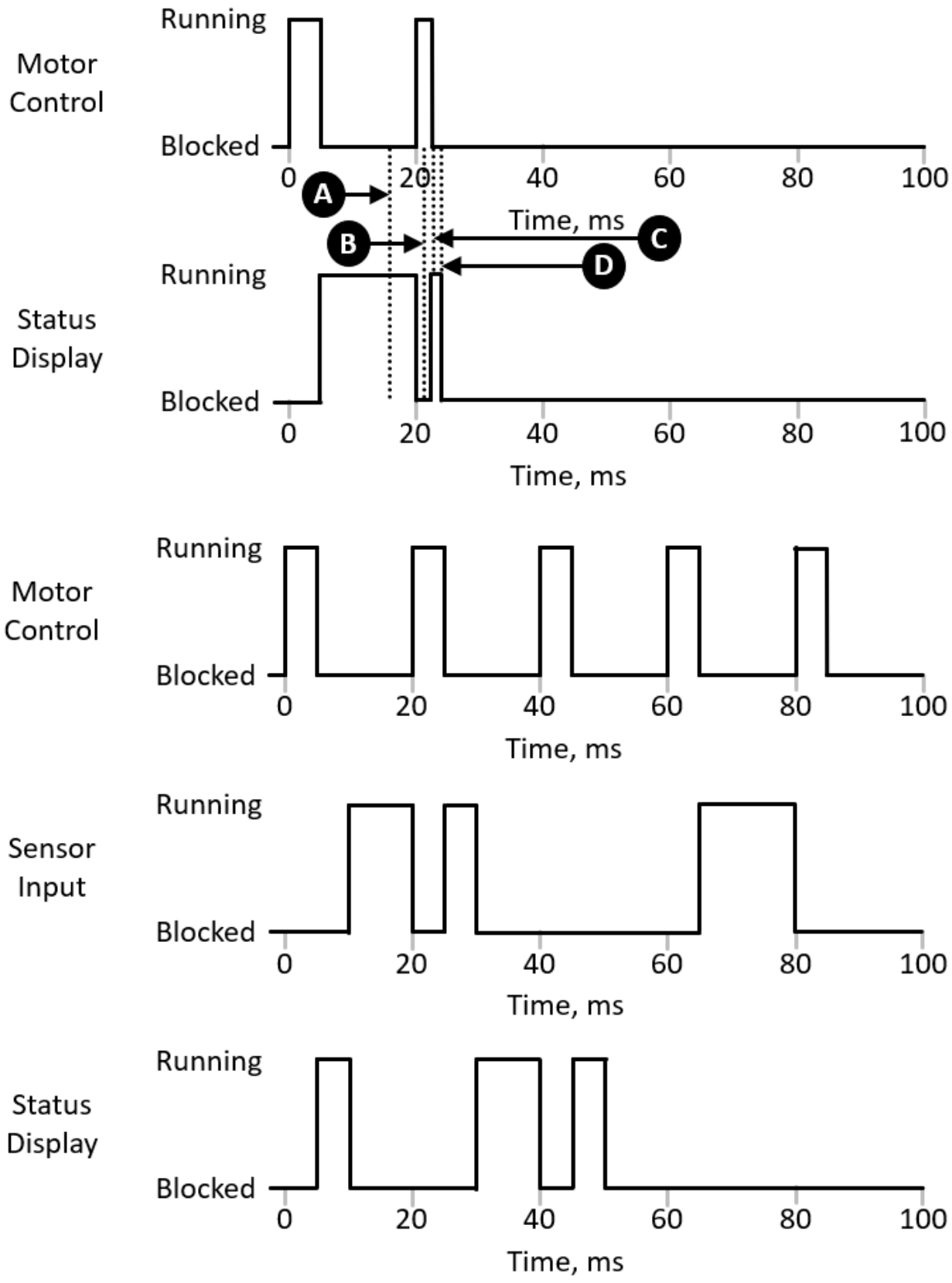

3.3V
3.3V
R1
4.7K
R2
4.7K
SCL
SDA
Micro-
Controller
(Master)
ADC
(Servant)
Temperature
Sensor
(Servant)
SCLK
MISO
MOSI
Micro-
Controller
(Master)
ADC
(Servant)
Temperature
Sensor
(Servant)
CS1
CS2

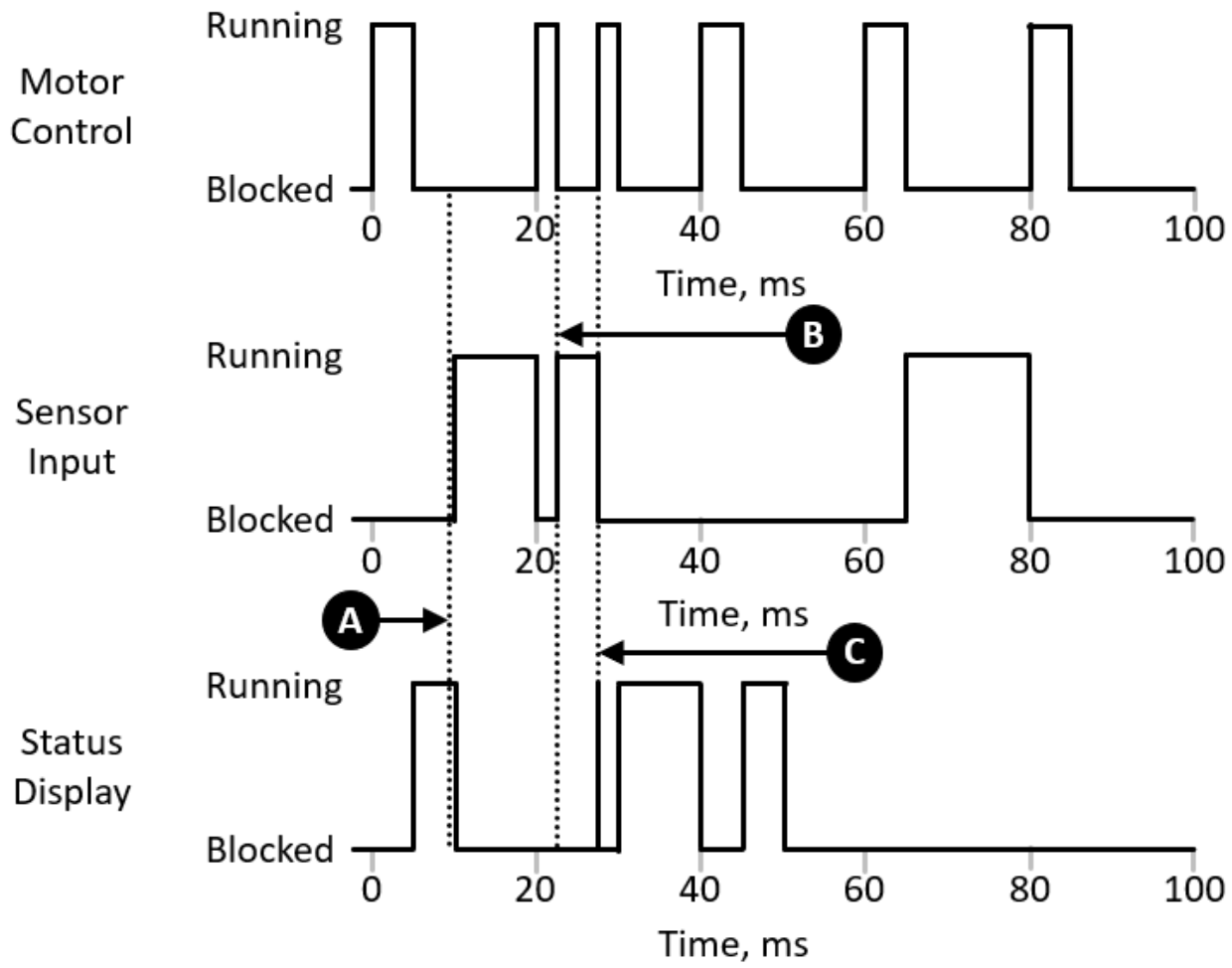

CAN_H
120 Ω
120 Ω
CAN_L
Micro-
Controller
ADC
Temperature
Sensor

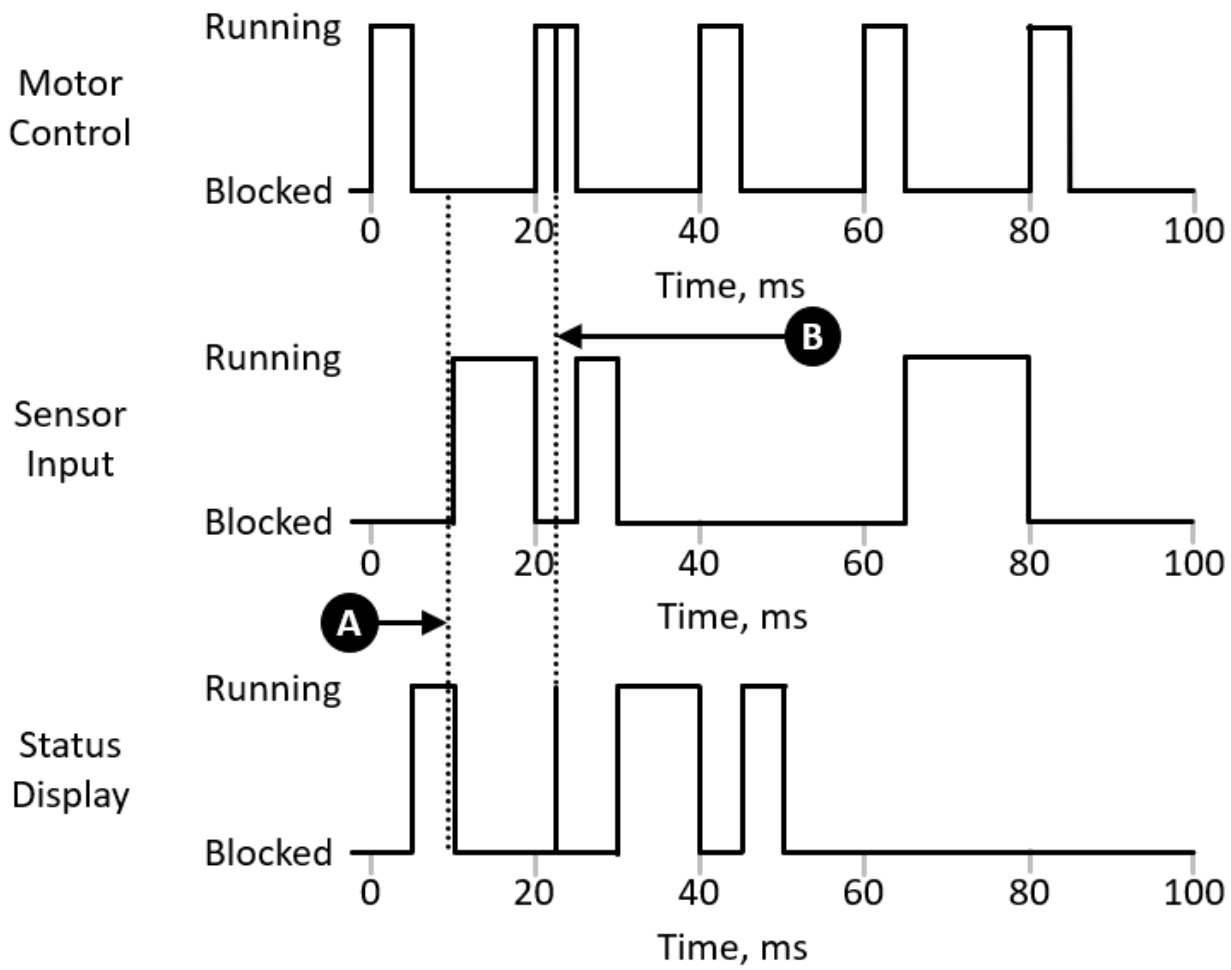
Chapter 3: Operating in Real Time



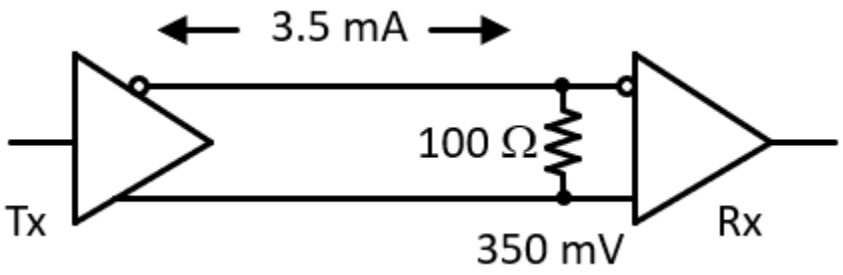

Motor Control
Running
Blocked
0
20
40
60
80
100
Time, ms
A
Status Display
Running
Blocked
0
20
40
60
80
100
Time, ms
Motor Control
Running
Blocked
0
A
20
40
60
80
100
Time, ms
B
C
Status Display
Running
Blocked
0
20
40
60
80
100
Time, ms

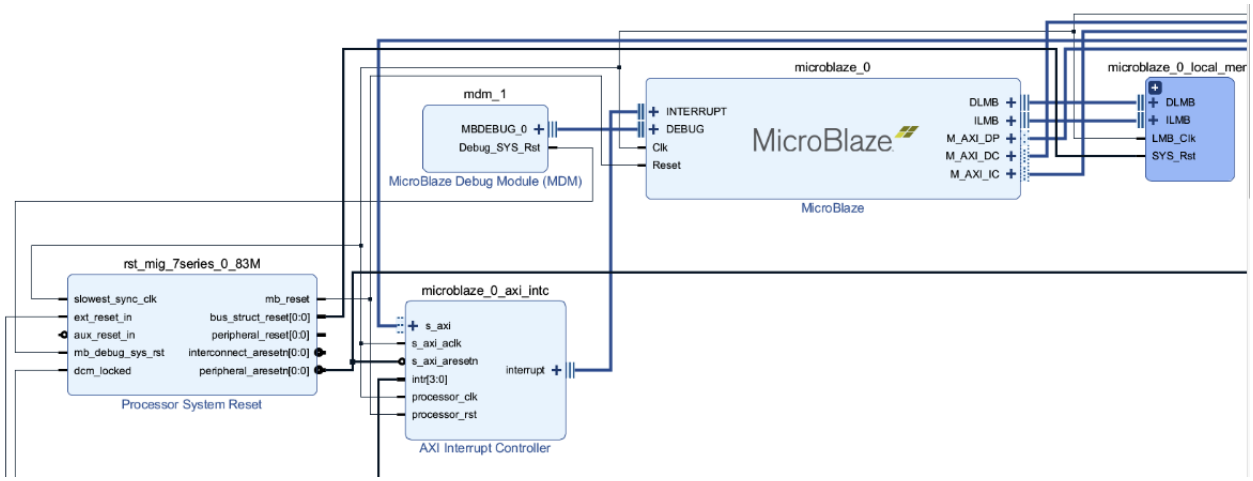

Motor Control
Running
Blocked
0
20
40
60
80
100
A
B
C
D
Time, ms
Status Display
Running
Blocked
0
20
40
60
80
100
Time, ms
Motor Control
Running
Blocked
0
20
40
60
80
100
Time, ms
Sensor Input
Running
Blocked
0
20
40
60
80
100
Time, ms
Status Display
Running
Blocked
0
20
40
60
80
100
Time, ms

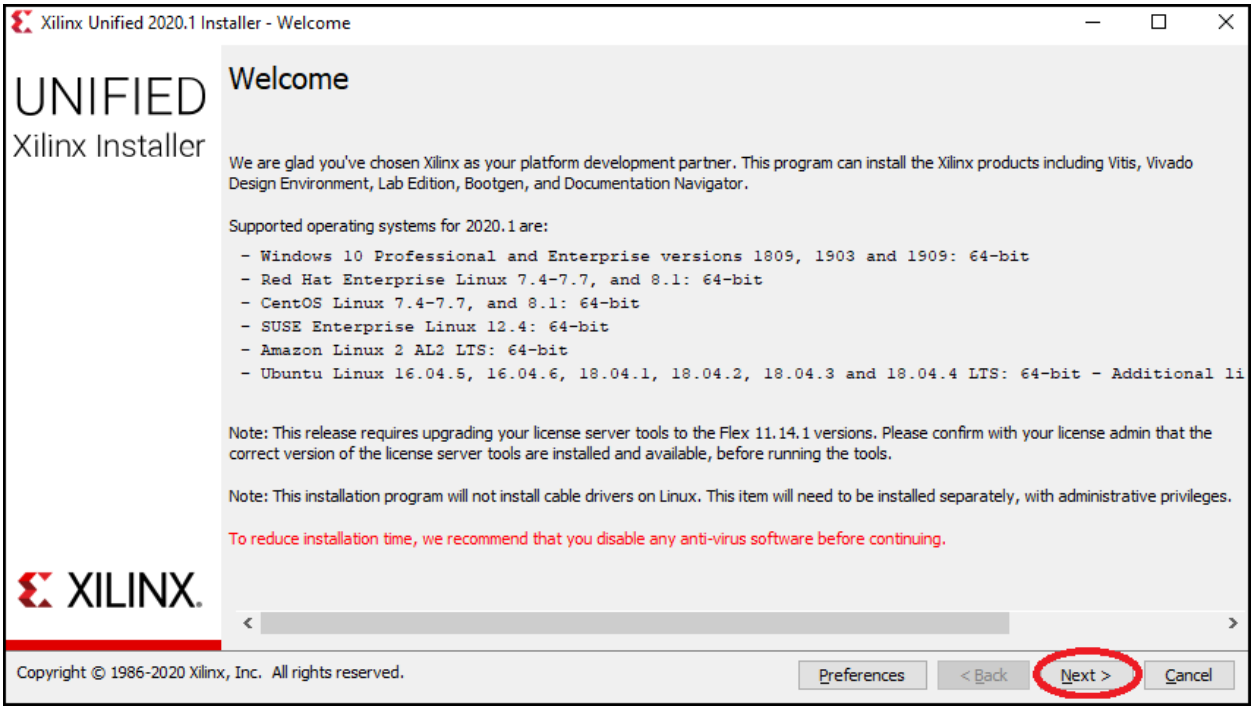

Motor Control
Running
Blocked
0
20
40
60
80
100
Time, ms
Sensor Input
Running
Blocked
B
0
20
40
60
80
100
Time, ms
A
C
Status Display
Running
Blocked
0
20
40
60
80
100
Time, ms

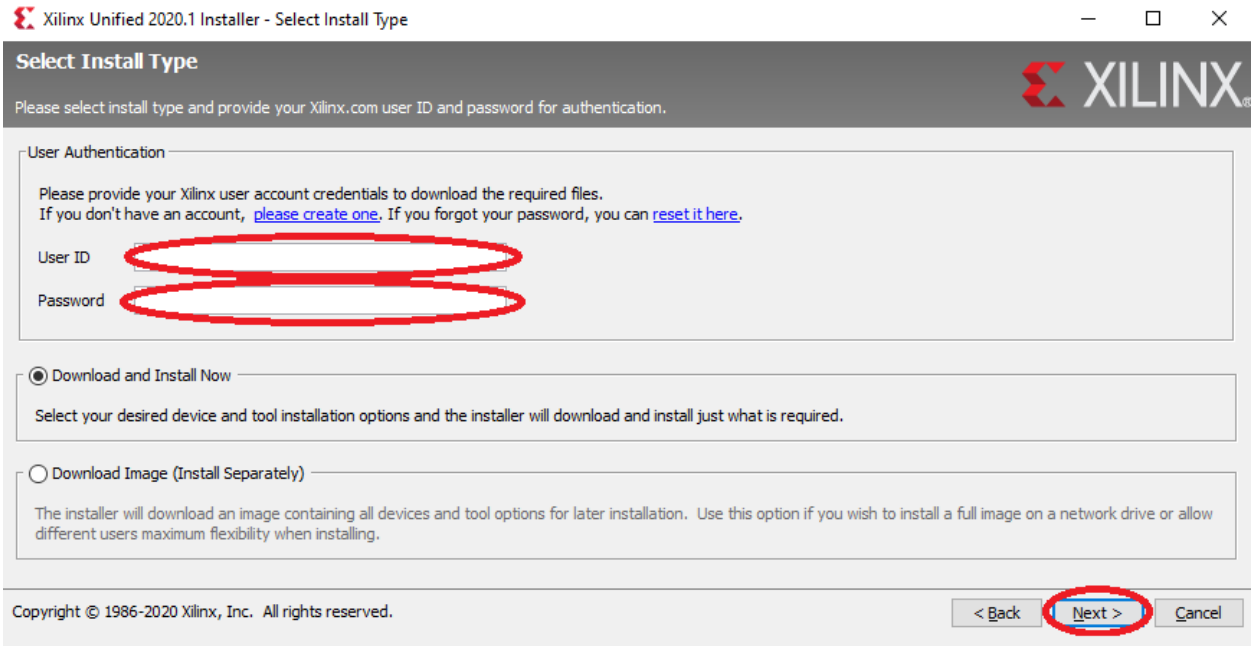

Motor Control
Running
Blocked
0
20
40
60
80
100
Time, ms
Sensor Input
Running
Blocked
B
A
Status Display
Running
Blocked

Chapter 4: Developing Your First FPGA Program








Xilinx Unified 2020.1 Installer - Select Install Type
Select Install Type
Please select install type and provide your Xilinx.com user ID and password for authentication.
XILINX
User Authentication
Please provide your Xilinx user account credentials to download the required files.
If you don't have an account, please create one. If you forgot your password, you can reset it here.
User ID
Password
Download and Install Now
Select your desired device and tool installation options and the installer will download and install just what is required.
Download Image (Install Separately)
The installer will download an image containing all devices and tool options for later installation. Use this option if you wish to install a full image on a network drive or allow different users maximum flexibility when installing.
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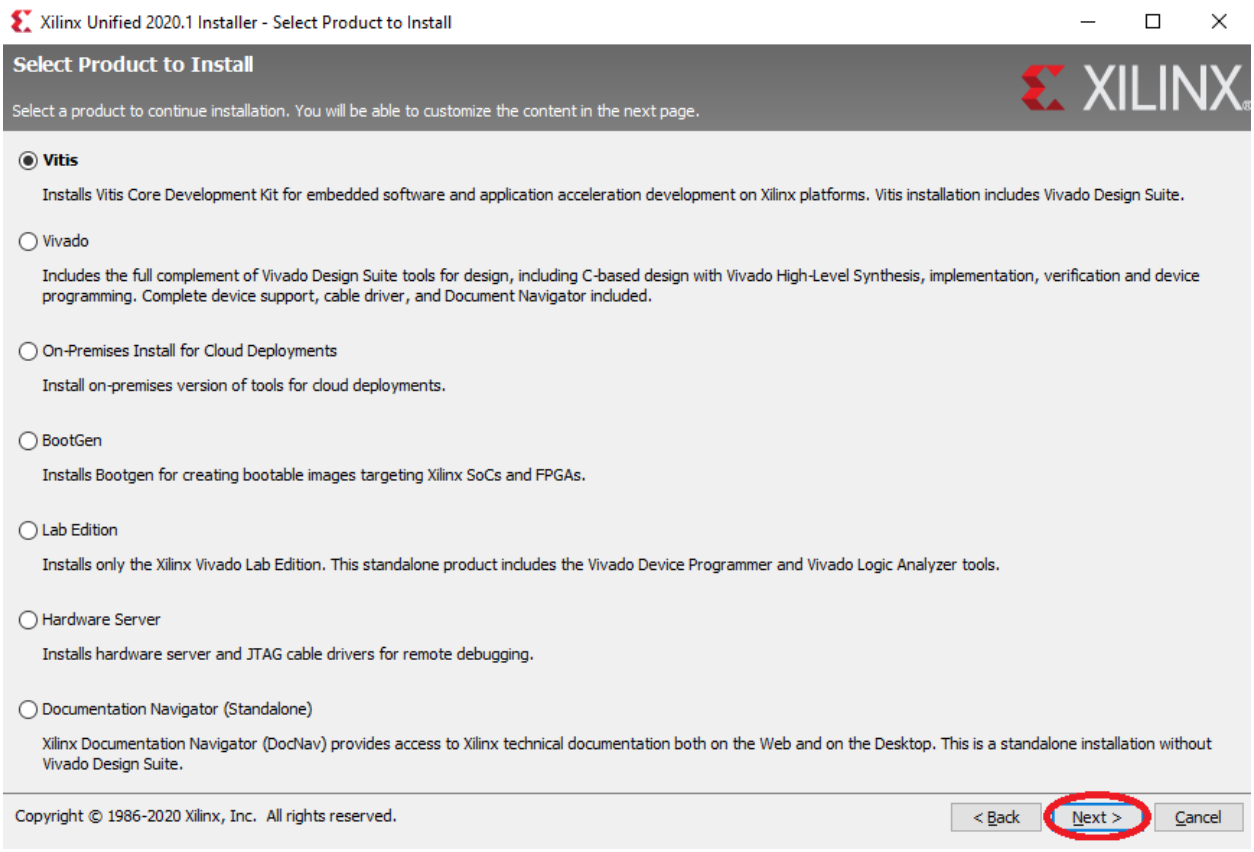
< Back
Next >
Cancel


Xilinx Unified 2020.1 Installer - Select Product to Install
Select Product to Install
Select a product to continue installation. You will be able to customize the content in the next page.
XILINX
Vitis
Installs Vitis Core Development Kit for embedded software and application acceleration development on Xilinx platforms. Vitis installation includes Vivado Design Suite.
Vivado
Includes the full complement of Vivado Design Suite tools for design, including C-based design with Vivado High-Level Synthesis, implementation, verification and device programming. Complete device support, cable driver, and Document Navigator included.
On-Premises Install for Cloud Deployments
Install on-premises version of tools for cloud deployments.
BootGen
Installs Bootgen for creating bootable images targeting Xilinx SoCs and FPGAs.
Lab Edition
Installs only the Xilinx Vivado Lab Edition. This standalone product includes the Vivado Device Programmer and Vivado Logic Analyzer tools.
Hardware Server
Installs hardware server and JTAG cable drivers for remote debugging.
Documentation Navigator (Standalone)
Xilinx Documentation Navigator (DocNav) provides access to Xilinx technical documentation both on the Web and on the Desktop. This is a standalone installation without Vivado Design Suite.
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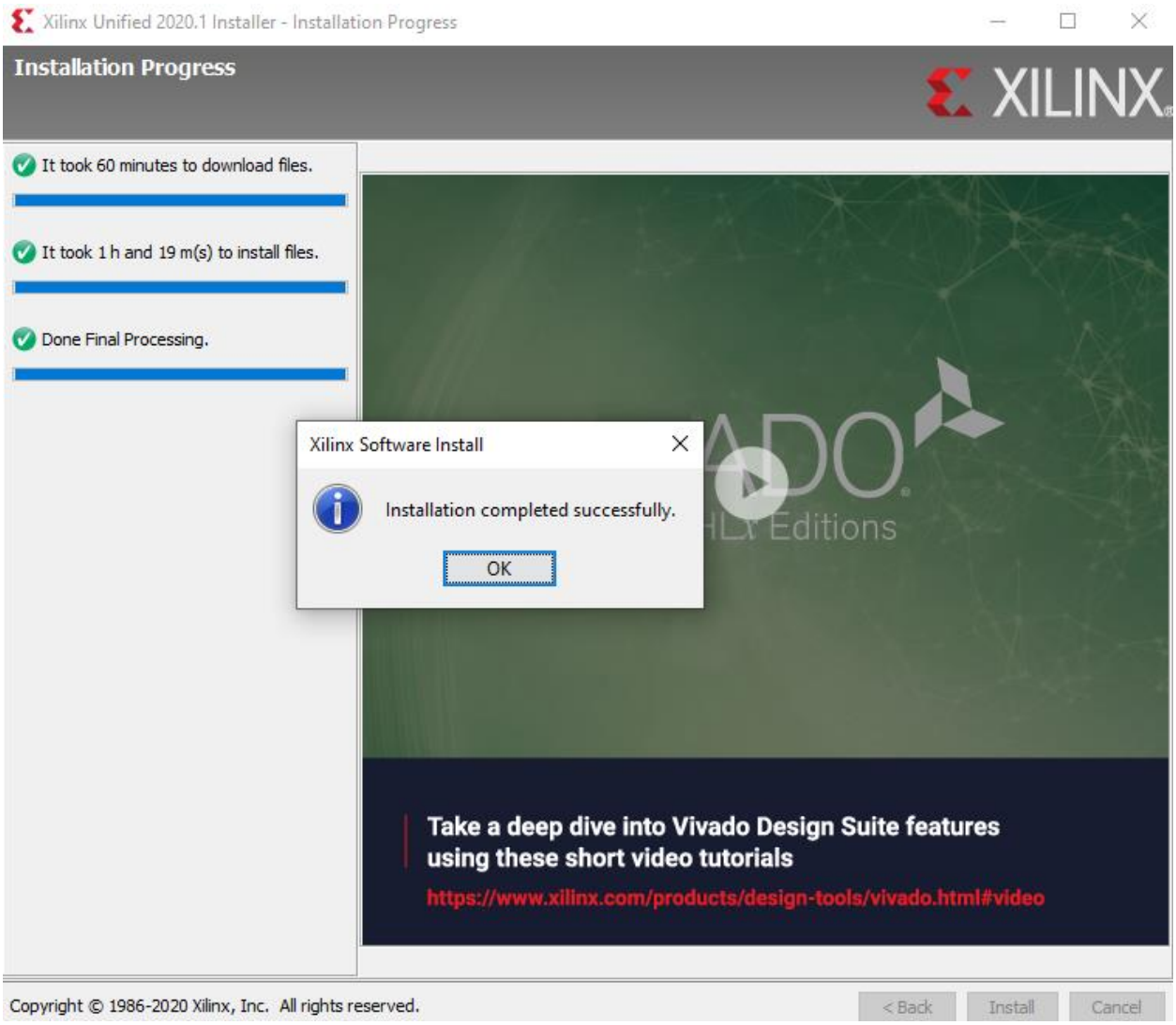
< Back
Next >
Cancel


Xilinx Unified 2020.1 Installer - Installation Progress
Installation Progress
XILINX
It took 60 minutes to download files.
It took 1 h and 19 m(s) to install files.
Done Final Processing.
Xilinx Software Install
Installation completed successfully.
OK
Editions
Take a deep dive into Vivado Design Suite features using these short video tutorials
https://www.xilinx.com/products/design-tools/vivado.html#video
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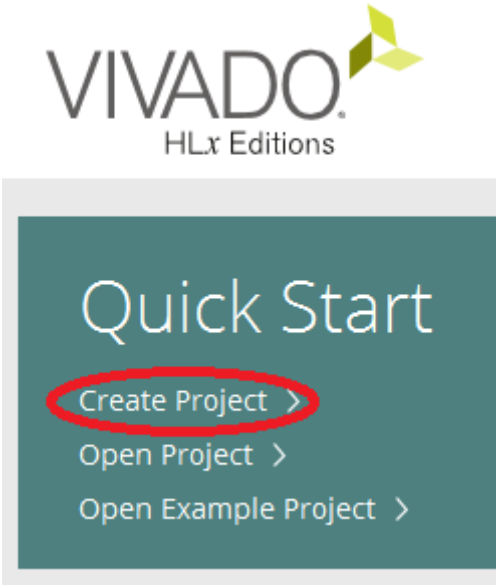
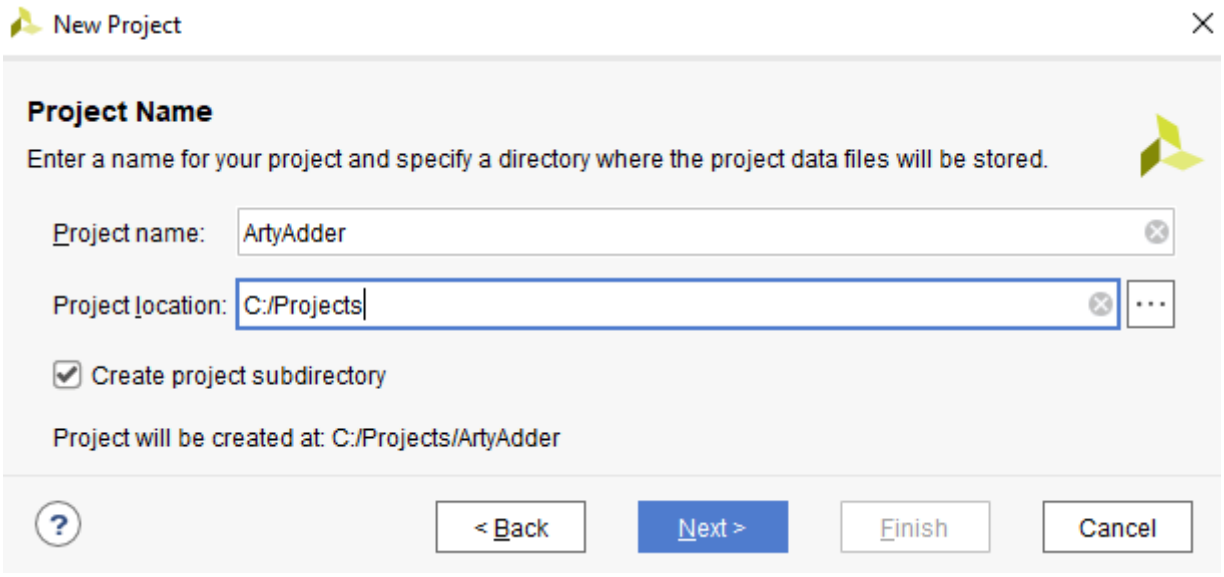
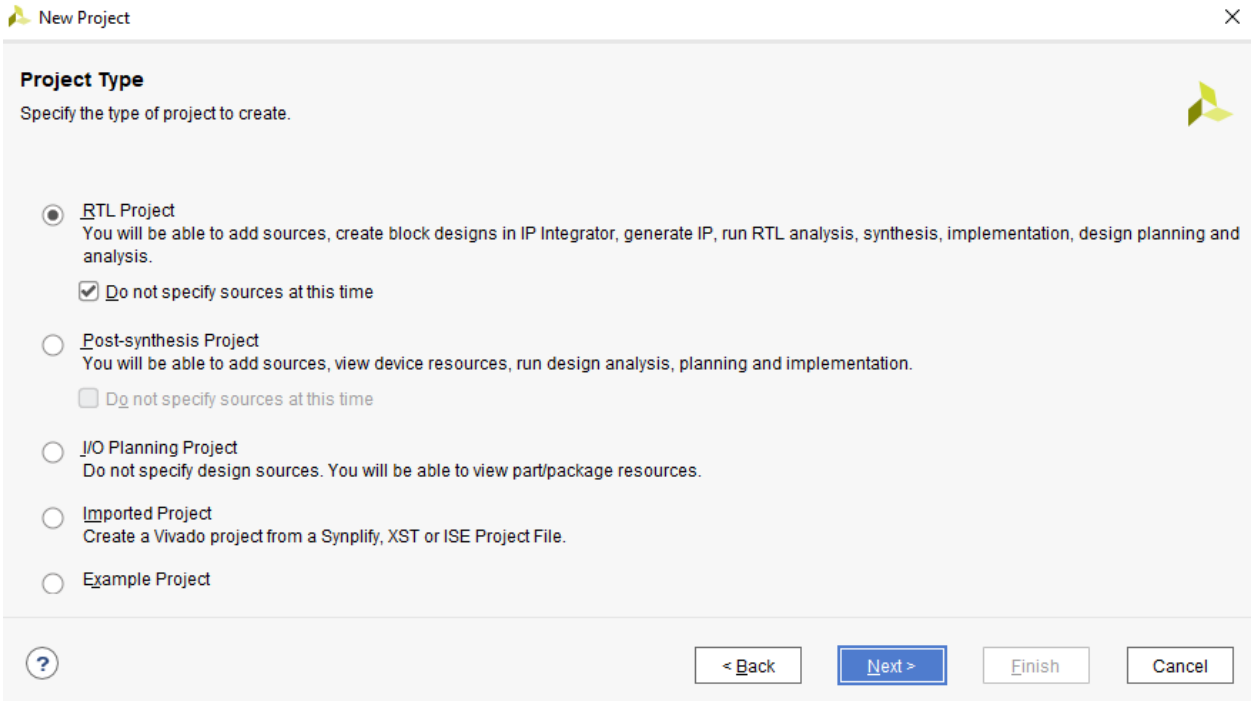
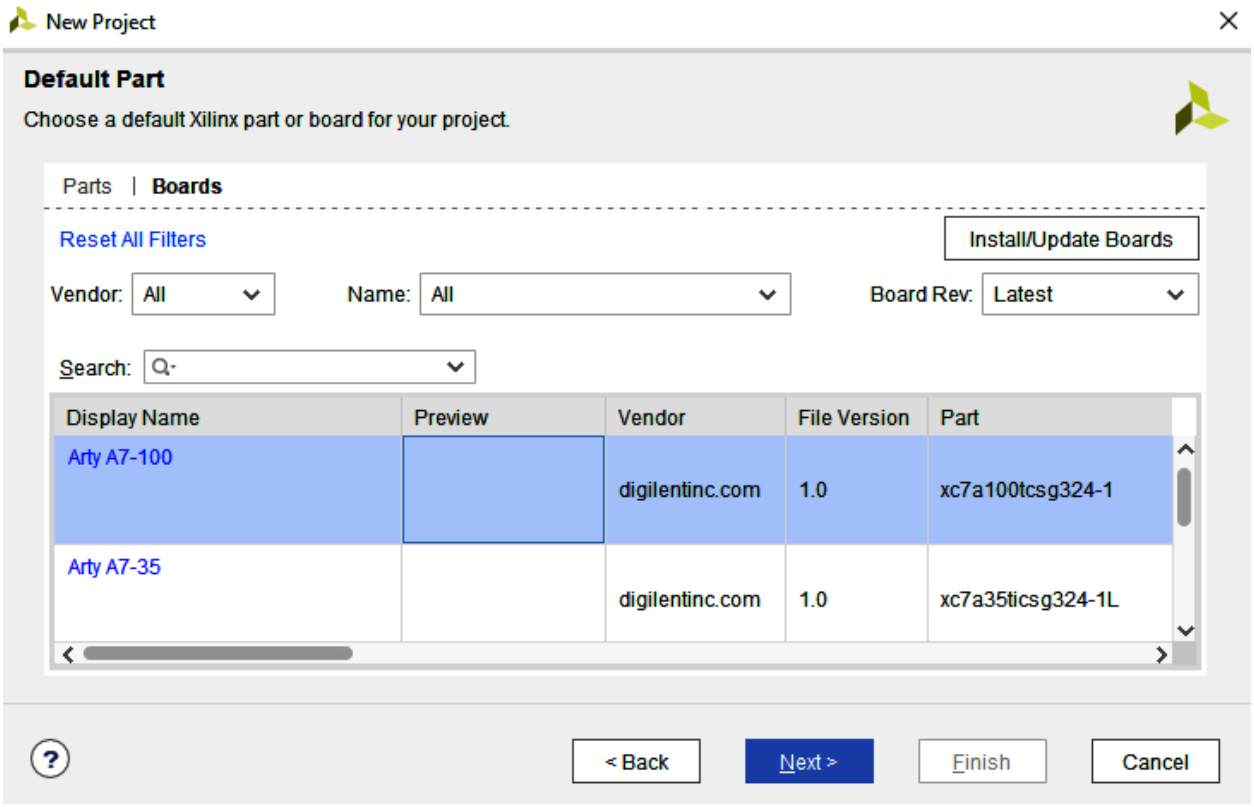
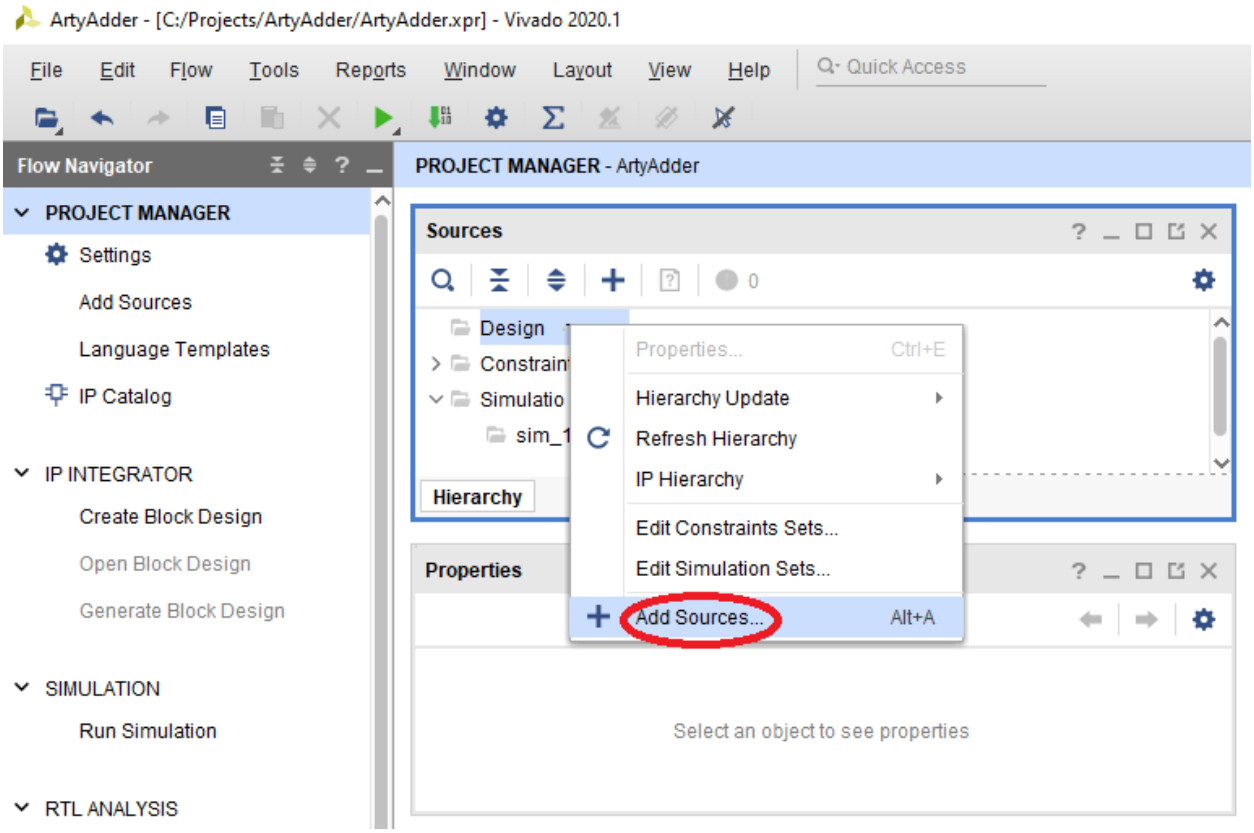
< Back
Install
Cancel

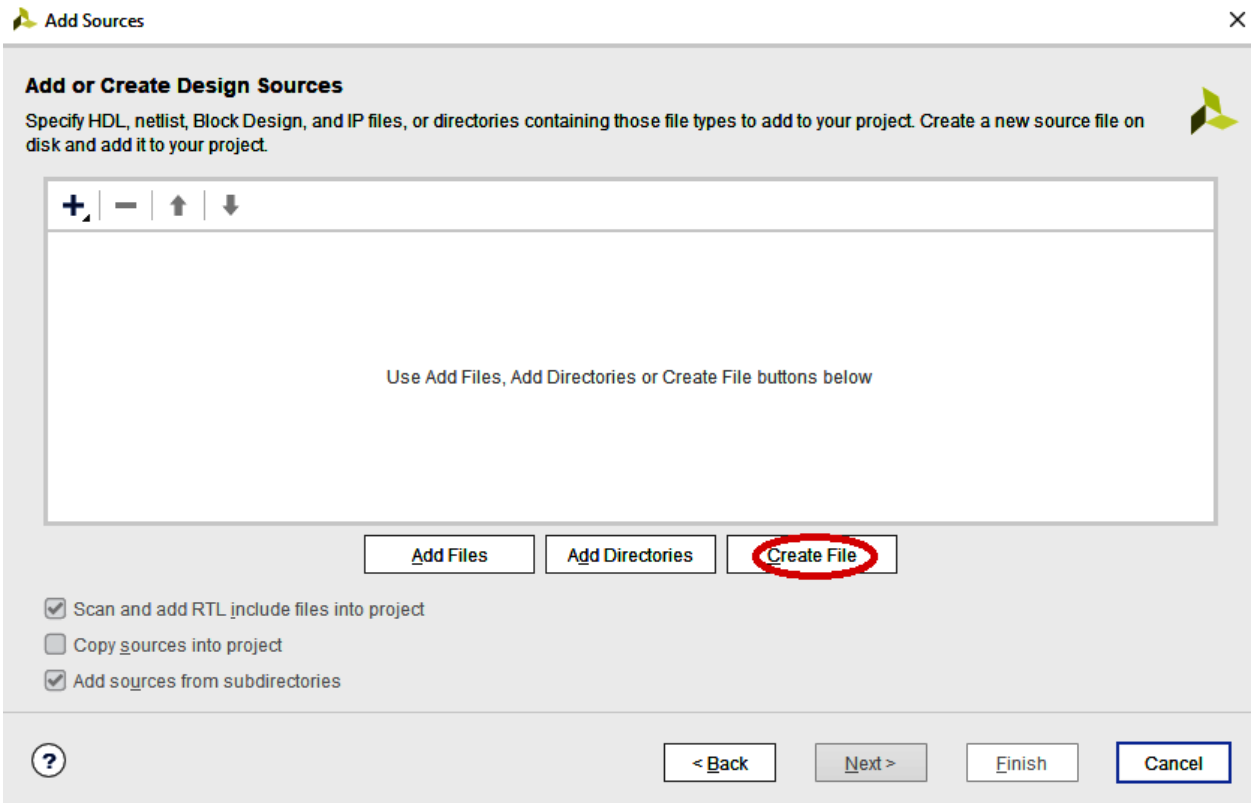

VIVADO
HLx Editions
Quick Start
Create Project
Open Project
Open Example Project

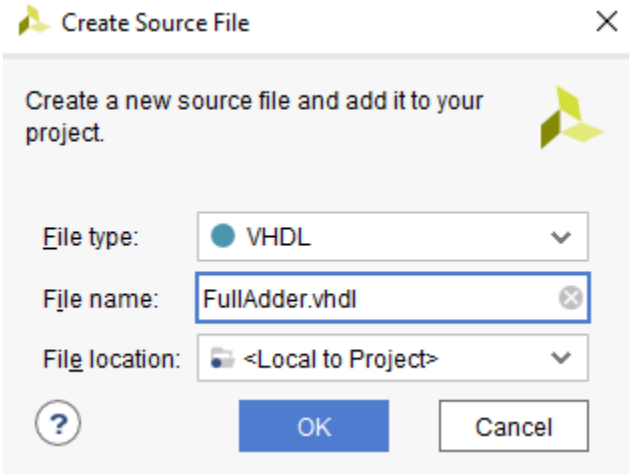

New Project
Project Name
Enter a name for your project and specify a directory where the project data files will be stored.
Project name:
ArtyAdder
Project location:
C:/Projects
Create project subdirectory
Project will be created at: C:/Projects/ArtyAdder
< Back
Next >
Finish
Cancel

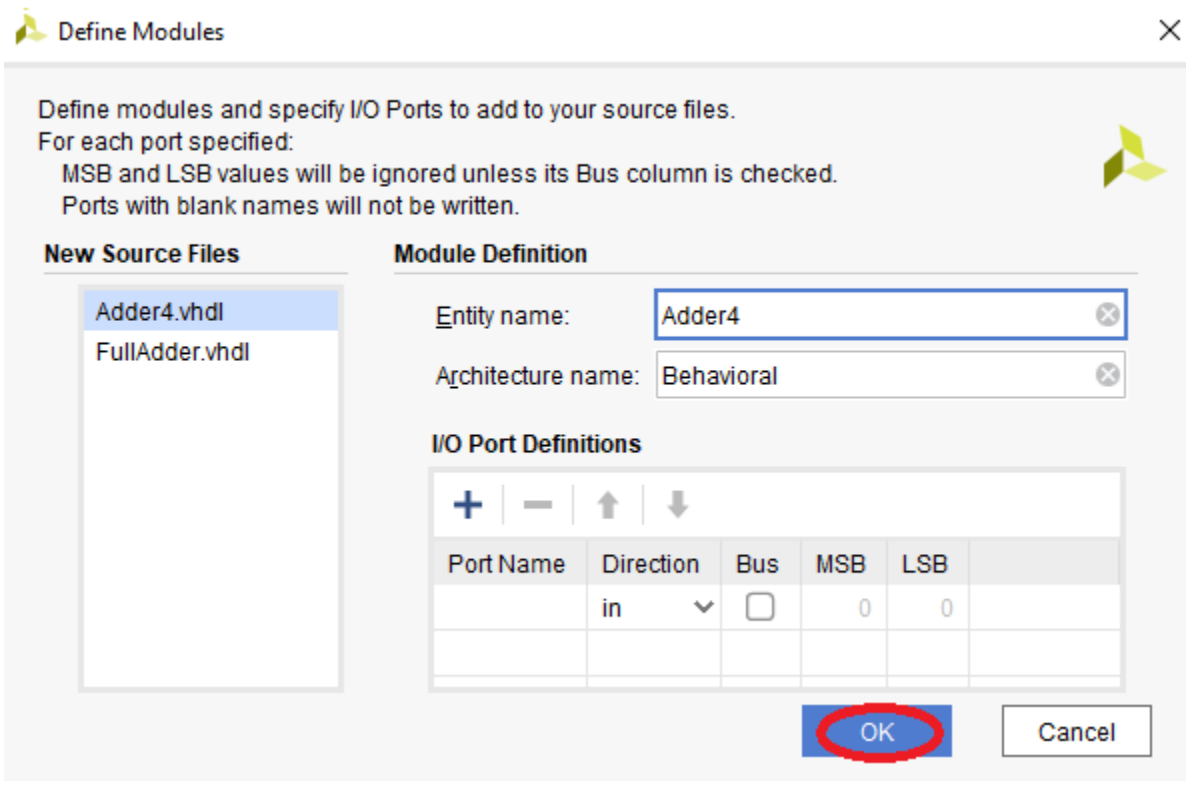

New Project
Project Type
Specify the type of project to create.
RTL Project
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
Do not specify sources at this time
Post-synthesis Project
You will be able to add sources, view device resources, run design analysis, planning and implementation.
Do not specify sources at this time
I/O Planning Project
Do not specify design sources. You will be able to view part/package resources.
Imported Project
Create a Vivado project from a Synplify, XST or ISE Project File.
Example Project
< Back
Next >
Finish
Cancel

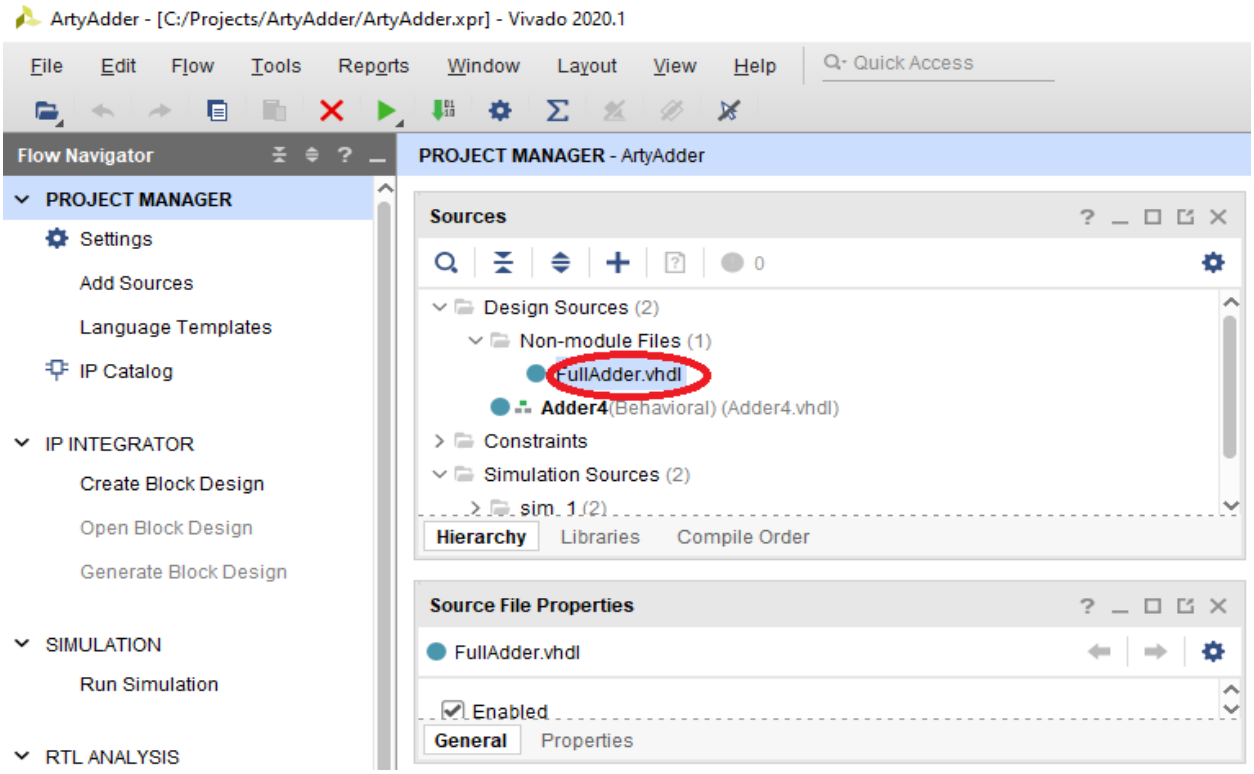

New Project
Default Part
Choose a default Xilinx part or board for your project.
Parts | Boards
Reset All Filters
Install/Update Boards
Vendor: All
Name: All
Board Rev: Latest
Search:
Display Name
Preview
Vendor
File Version
Part
Arty A7-100
digilentinc.com
1.0
xc7a100tcsg324-1
Arty A7-35
digilentinc.com
1.0
xc7a35ticsg324-1L
< Back
Next >
Finish
Cancel

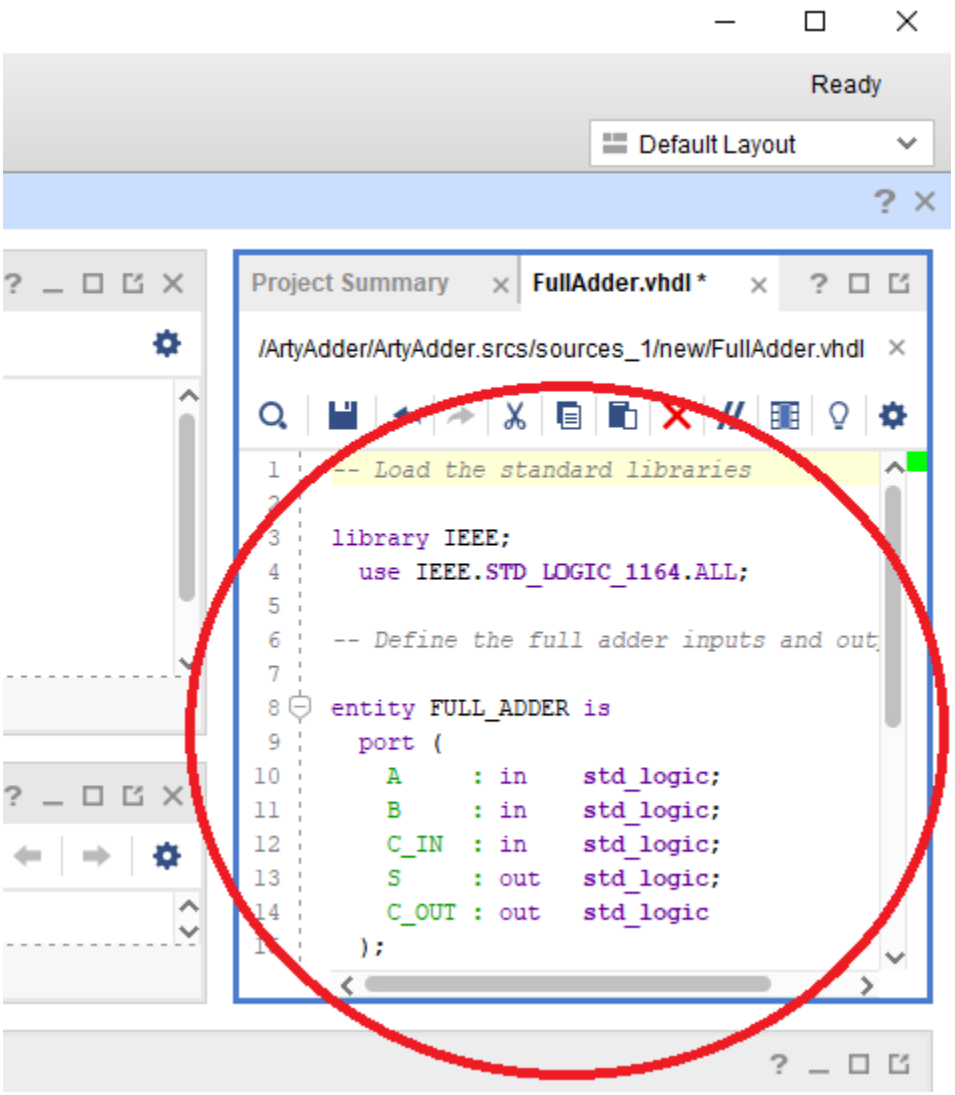

ArtyAdder - [C:/Projects/ArtyAdder/ArtyAdder.xpr] - Vivado 2020.1
File
Edit
Flow
Tools
Reports
Window
Layout
View
Help
Quick Access
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
PROJECT MANAGER - ArtyAdder
Sources
Design
Constraint
Simulatio
sim_1
Hierarchy
Properties...
Ctrl+E
Hierarchy Update
Refresh Hierarchy
IP Hierarchy
Edit Constraints Sets...
Edit Simulation Sets...
Add Sources...
Alt+A
Properties
Select an object to see properties

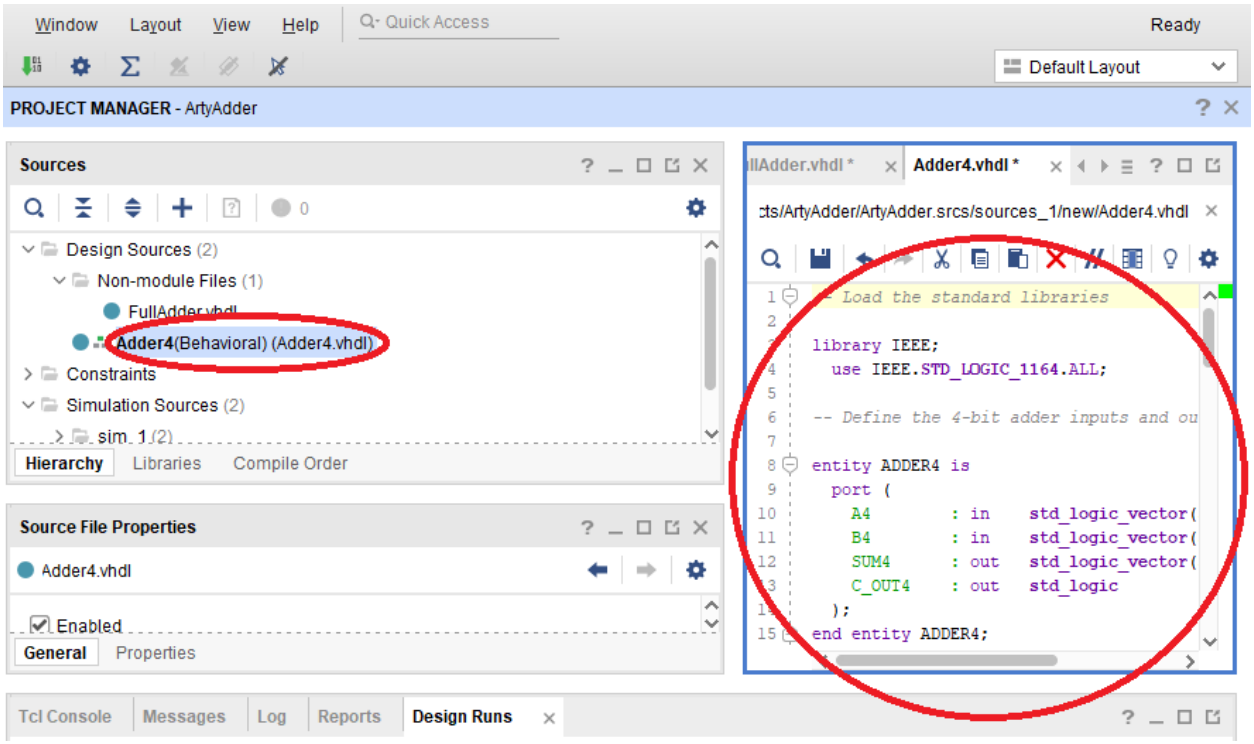

Add Sources
Add or Create Design Sources
Specify HDL, netlist, Block Design, and IP files, or directories containing those file types to add to your project. Create a new source file on disk and add it to your project.
Use Add Files, Add Directories or Create File buttons below
Add Files
Add Directories
Create File
Scan and add RTL include files into project
Copy sources into project
Add sources from subdirectories
< Back
Next >
Finish
Cancel

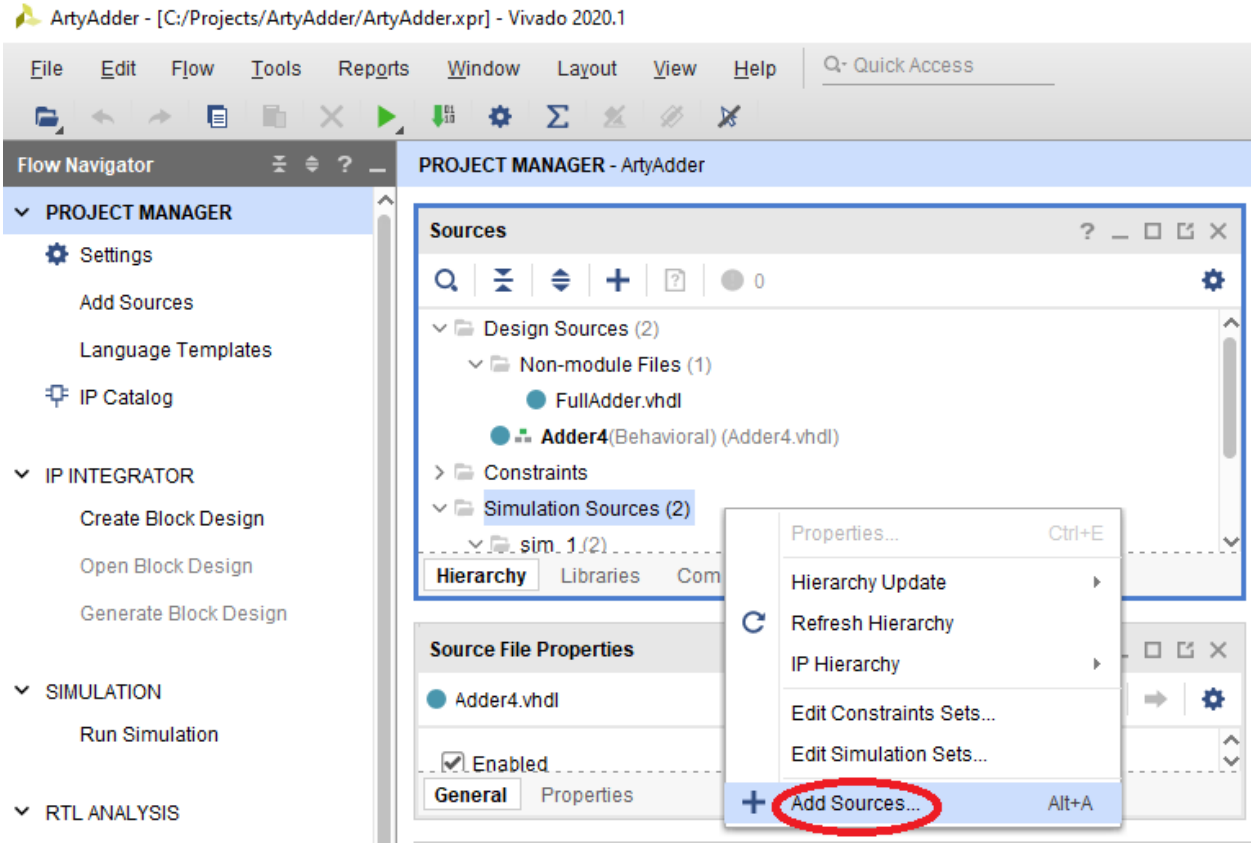

Create Source File
Create a new source file and add it to your project.
File type:
VHDL
File name:
FullAdder.vhdl
File location:
<Local to Project>
OK
Cancel

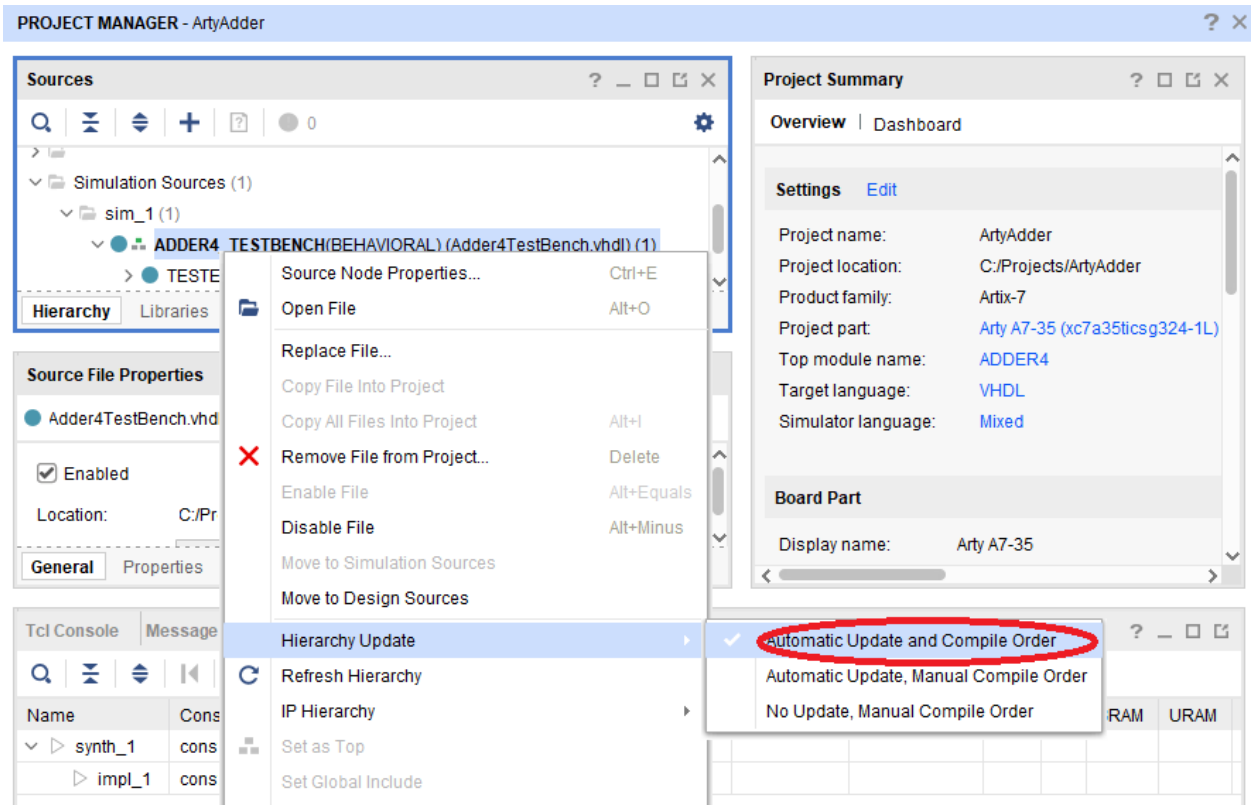

Define Modules
Define modules and specify I/O Ports to add to your source files.
For each port specified:
MSB and LSB values will be ignored unless its Bus column is checked.
Ports with blank names will not be written.
New Source Files
Adder4.vhdl
FullAdder.vhdl
Module Definition
Entity name:
Adder4
Architecture name:
Behavioral
I/O Port Definitions
Port Name
Direction
Bus
MSB
LSB
in
0
0
OK
Cancel

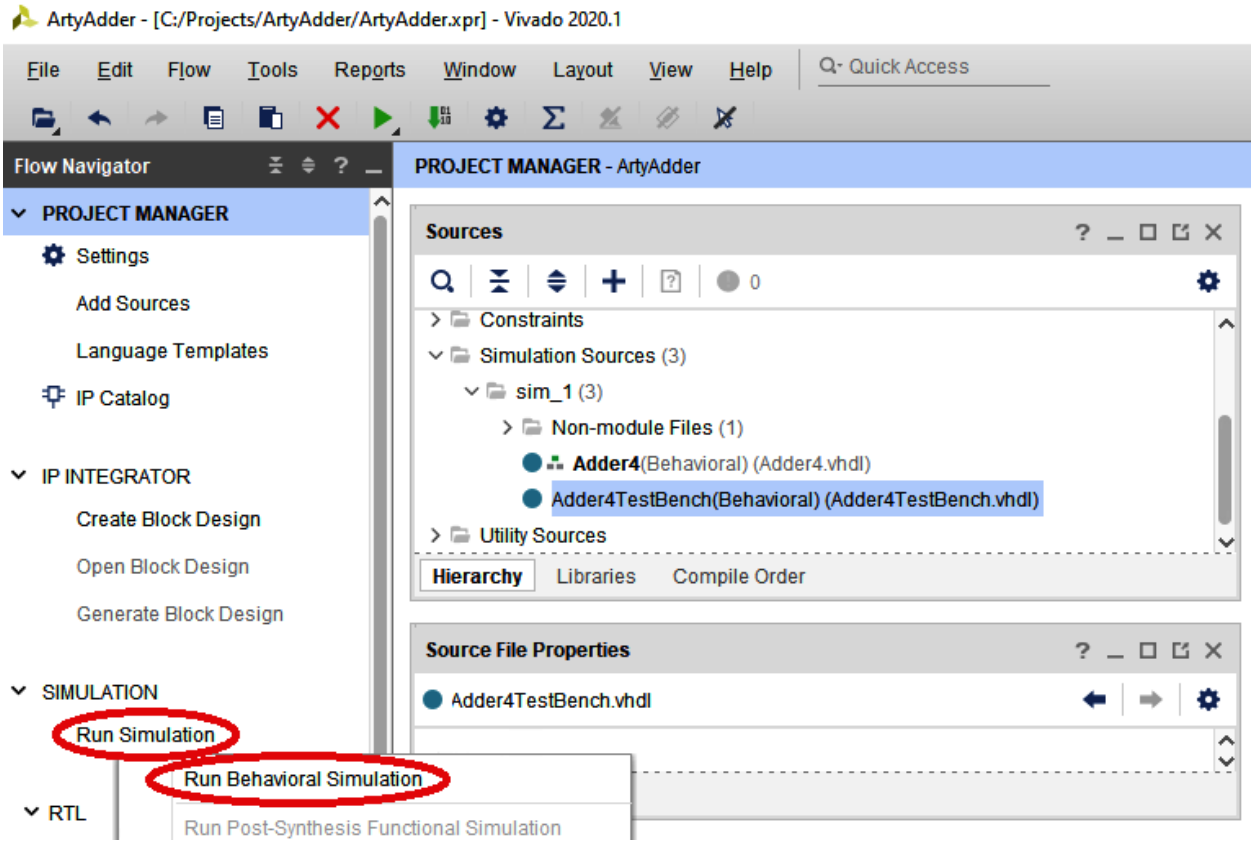

ArtyAdder - [C:/Projects/ArtyAdder/ArtyAdder.xpr] - Vivado 2020.1
File
Edit
Flow
Tools
Reports
Window
Layout
View
Help
Quick Access
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
PROJECT MANAGER - ArtyAdder
Sources
Design Sources (2)
Non-module Files (1)
FullAdder.vhdl
Adder4(Behavioral) (Adder4.vhdl)
Constraints
Simulation Sources (2)
sim_1 (2)
Hierarchy
Libraries
Compile Order
Source File Properties
FullAdder.vhdl
Enabled
General
Properties

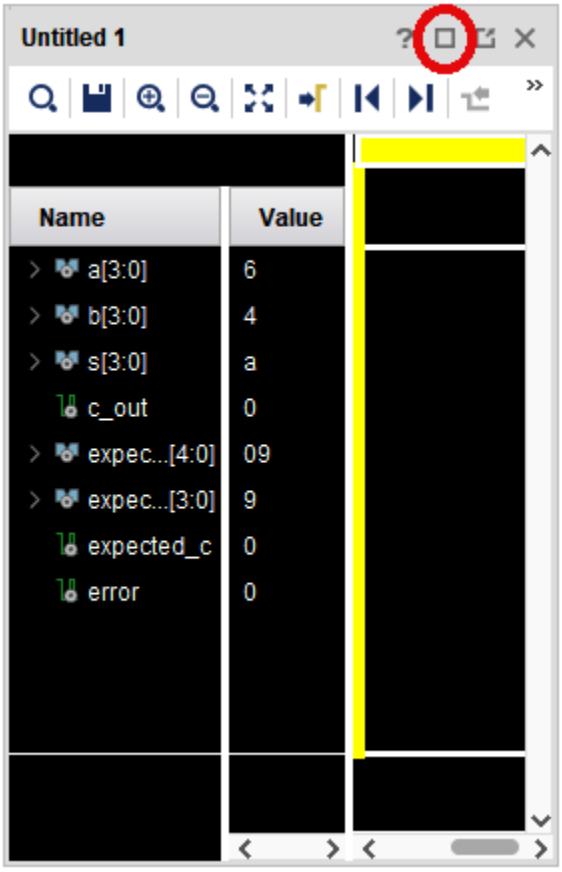

Ready
Default Layout
Project Summary
FullAdder.vhdl *
/ArtyAdder/ArtyAdder.srcs/sources_1/new/FullAdder.vhdl
1 -- Load the standard libraries
3 library IEEE;
4 use IEEE.STD_LOGIC_1164.ALL;
6 -- Define the full adder inputs and out
8 entity FULL_ADDER is
9 port (
10 A : in std_logic;
11 B : in std_logic;
12 C_IN : in std_logic;
13 S : out std_logic;
14 C_OUT : out std_logic
);

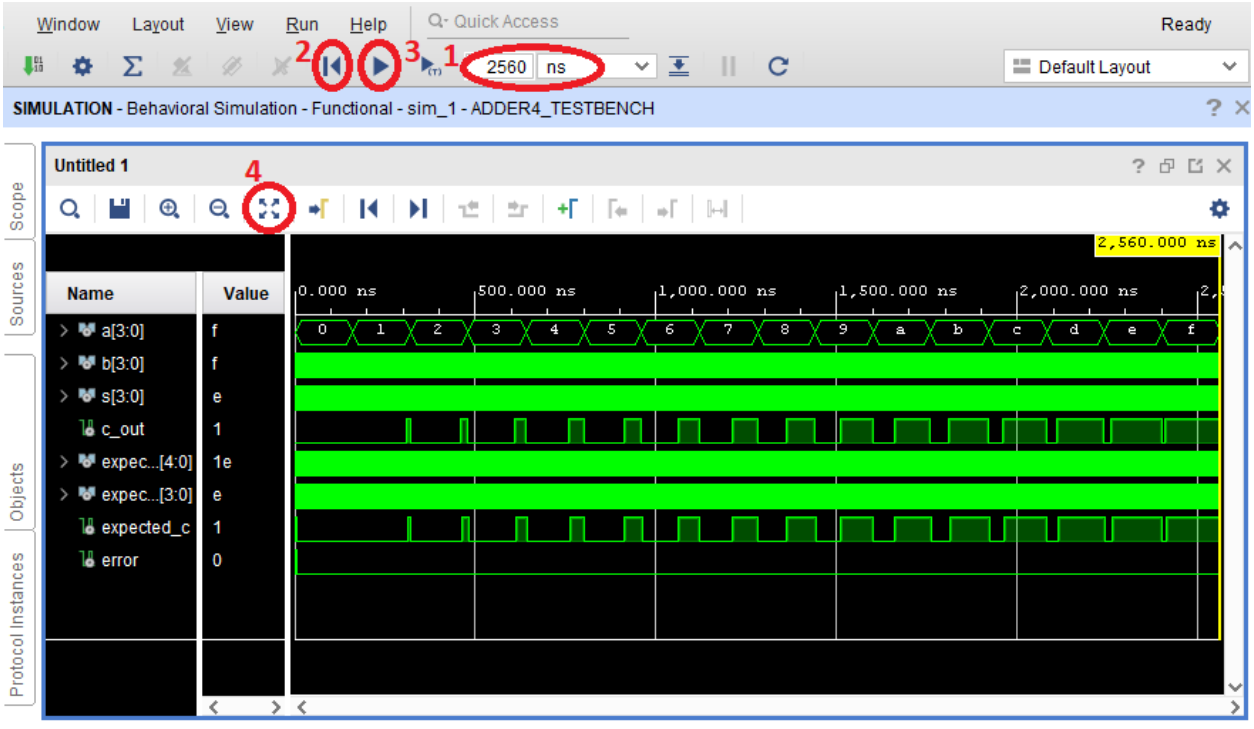

Window
Layout
View
Help
Quick Access
Ready
Default Layout
PROJECT MANAGER - ArtyAdder
Sources
Design Sources (2)
Non-module Files (1)
FullAdder.vhdl
Adder4(Behavioral) (Adder4.vhdl)
Constraints
Simulation Sources (2)
sim_1 (2)
Hierarchy
Libraries
Compile Order
Source File Properties
Adder4.vhdl
Enabled
General
Properties
Adder4.vhdl *
cts/ArtyAdder/ArtyAdder.srcs/sources_1/new/Adder4.vhdl
-- Load the standard libraries
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
-- Define the 4-bit adder inputs and ou
entity ADDER4 is
port (
A4 : in std_logic_vector(
B4 : in std_logic_vector(
SUM4 : out std_logic_vector(
C_OUT4 : out std_logic
);
end entity ADDER4;
Tcl Console
Messages
Log
Reports
Design Runs

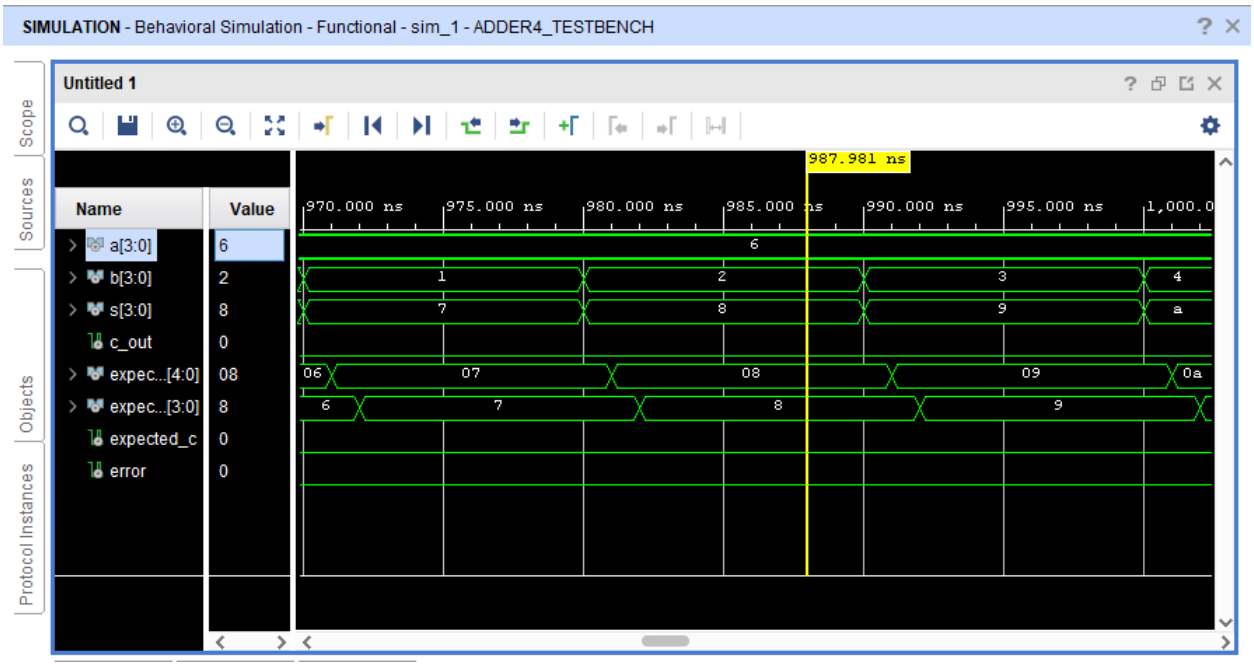

ArtyAdder - [C:/Projects/ArtyAdder/ArtyAdder.xpr] - Vivado 2020.1
File
Edit
Flow
Tools
Reports
Window
Layout
View
Help
Quick Access
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
PROJECT MANAGER - ArtyAdder
Sources
Design Sources (2)
Non-module Files (1)
FullAdder.vhdl
Adder4(Behavioral) (Adder4.vhdl)
Constraints
Simulation Sources (2)
sim_1 (2)
Hierarchy
Libraries
Source File Properties
Adder4.vhdl
Enabled
General
Properties
Properties... Ctrl+E
Hierarchy Update
Refresh Hierarchy
IP Hierarchy
Edit Constraints Sets...
Edit Simulation Sets...
Add Sources... Alt+A

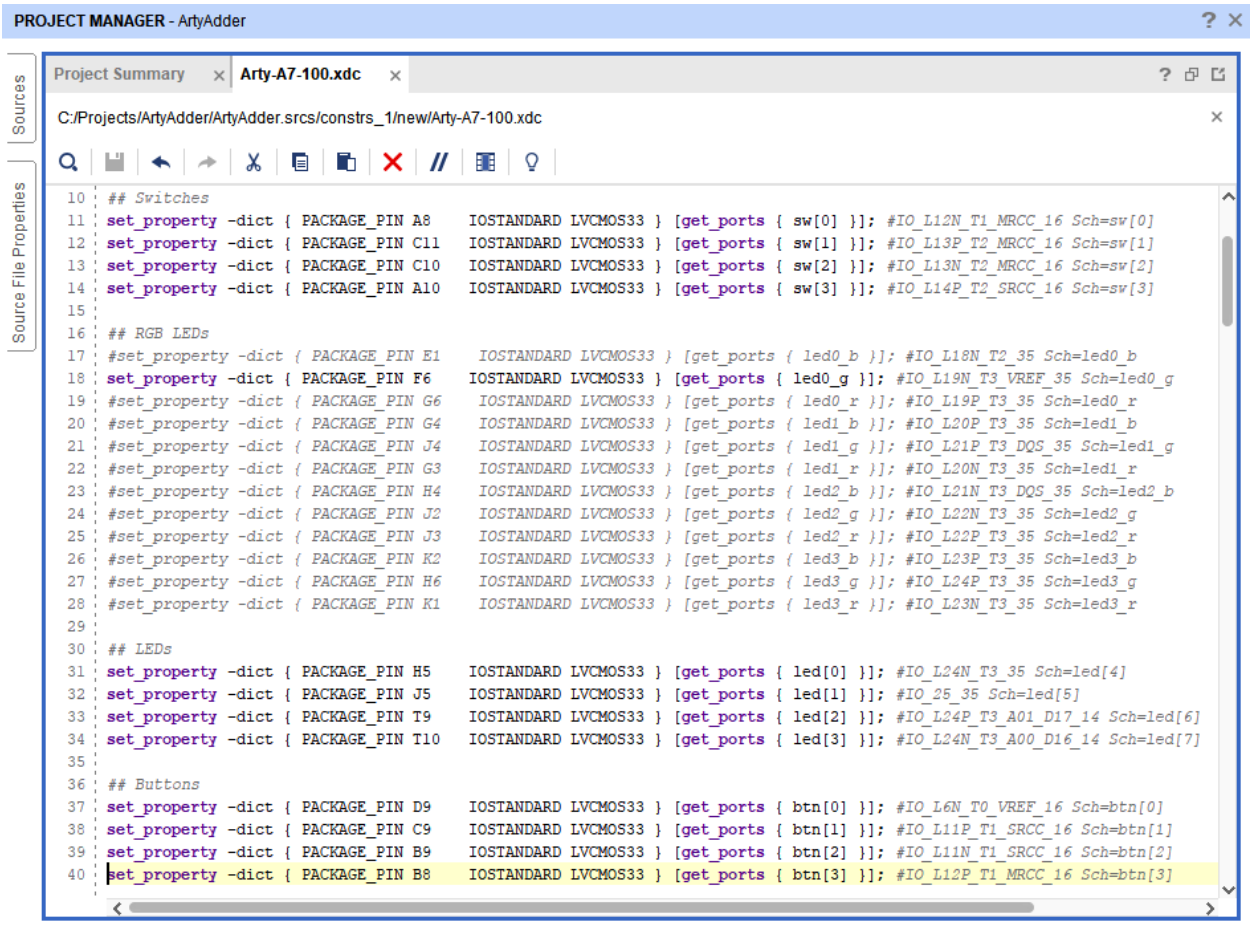

PROJECT MANAGER - ArtyAdder
Sources
Simulation Sources (1)
sim_1 (1)
ADDER4_TESTBENCH(BEHAVIORAL) (Adder4TestBench.vhdl) (1)
Hierarchy
Libraries
Source File Properties
Adder4TestBench.vhd
Enabled
Location:
General
Properties
Source Node Properties... Ctrl+E
Open File Alt+O
Replace File...
Copy File Into Project
Copy All Files Into Project Alt+I
Remove File from Project... Delete
Enable File Alt+Equals
Disable File Alt+Minus
Move to Simulation Sources
Move to Design Sources
Hierarchy Update
Refresh Hierarchy
IP Hierarchy
Set as Top
Set Global Include
Automatic Update and Compile Order
Automatic Update, Manual Compile Order
No Update, Manual Compile Order
Project Summary
Overview | Dashboard
Settings Edit
Project name: ArtyAdder
Project location: C:/Projects/ArtyAdder
Product family: Artix-7
Project part: Arty A7-35 (xc7a35ticsg324-1L)
Top module name: ADDER4
Target language: VHDL
Simulator language: Mixed
Board Part
Display name: Arty A7-35
Tcl Console
Message
Name
Cons
synth_1
impl_1
RAM
URAM

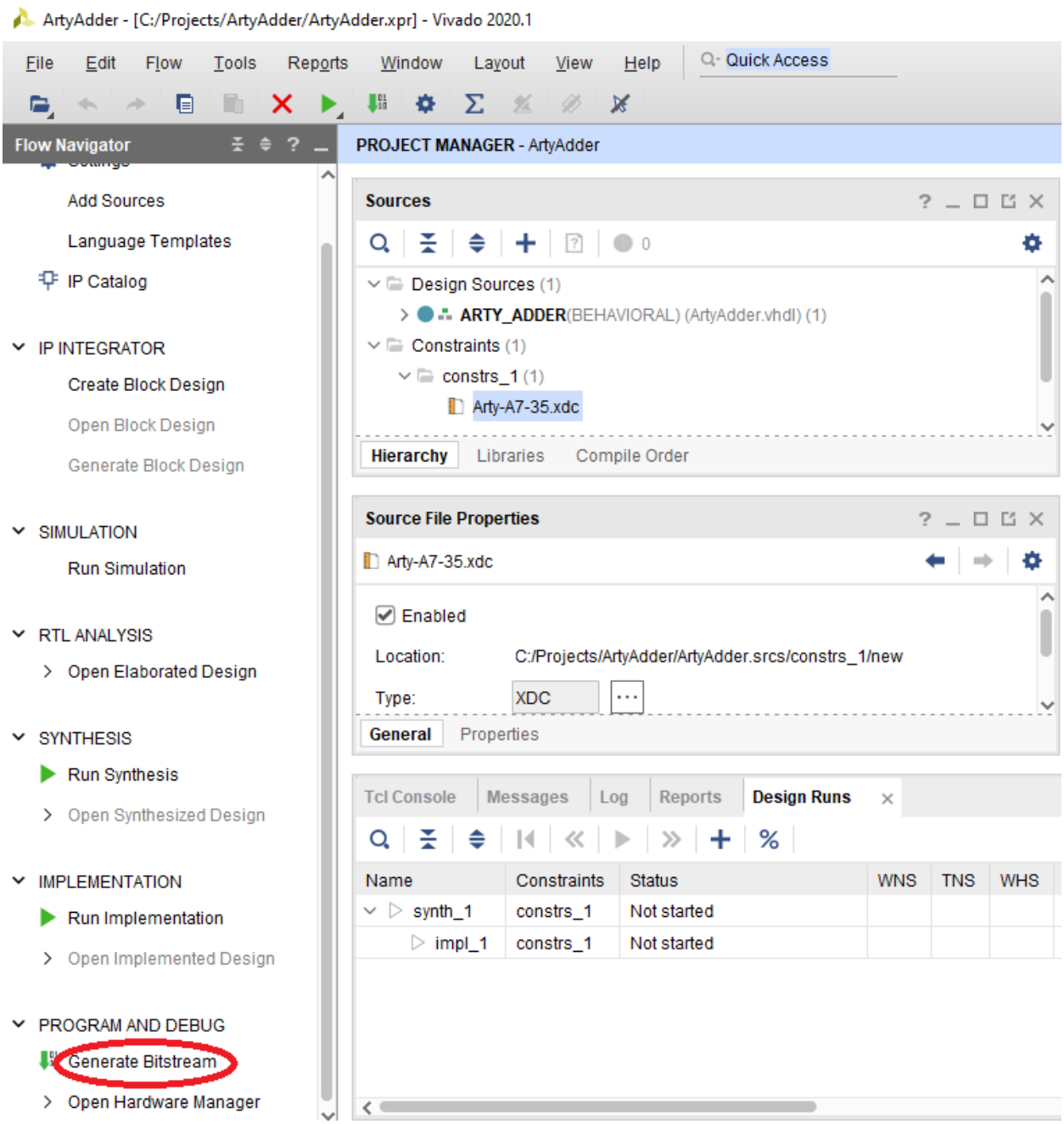

ArtyAdder - [C:/Projects/ArtyAdder/ArtyAdder.xpr] - Vivado 2020.1
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
Run Behavioral Simulation
Run Post-Synthesis Functional Simulation
RTL
PROJECT MANAGER - ArtyAdder
Sources
Constraints
Simulation Sources (3)
sim_1 (3)
Non-module Files (1)
Adder4(Behavioral) (Adder4.vhdl)
Adder4TestBench(Behavioral) (Adder4TestBench.vhdl)
Utility Sources
Hierarchy
Libraries
Compile Order
Source File Properties
Adder4TestBench.vhdl

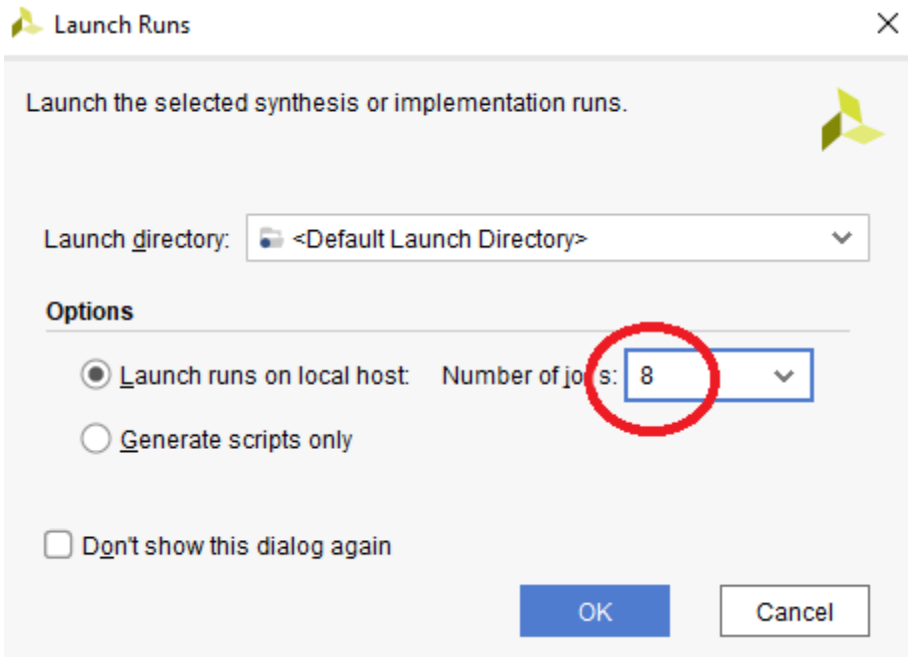

Untitled 1
Name
Value
a[3:0]
6
b[3:0]
4
s[3:0]
a
c_out
0
expec...[4:0]
09
expec...[3:0]
9
expected_c
0
error
0

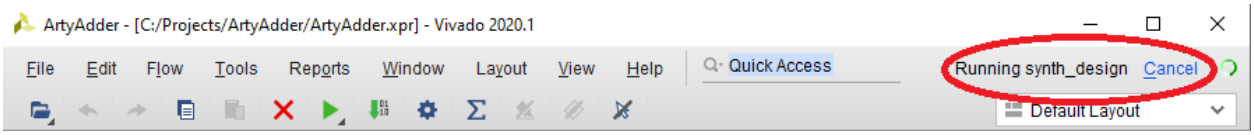

Window
Layout
View
Run
Help
Quick Access
Ready
2
3
1
2560
ns
Default Layout
SIMULATION - Behavioral Simulation - Functional - sim_1 - ADDER4_TESTBENCH
Untitled 1
4
Scope
Sources
Objects
Protocol Instances
Name
Value
a[3:0]
f
b[3:0]
f
s[3:0]
e
c_out
1
expec...[4:0]
1e
expec...[3:0]
e
expected_c
1
error
0
2,560.000 ns
0.000 ns
500.000 ns
1,000.000 ns
1,500.000 ns
2,000.000 ns
0
1
2
3
4
5
6
7
8
9
a
b
c
d
e
f

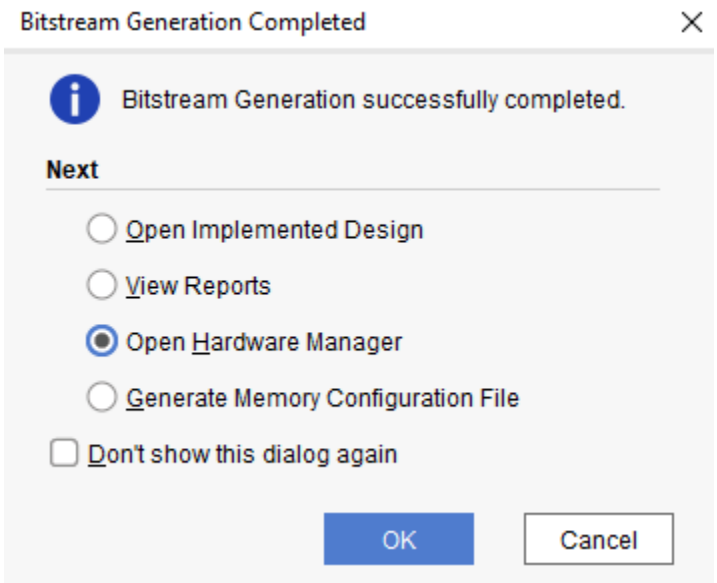

SIMULATION - Behavioral Simulation - Functional - sim_1 - ADDER4_TESTBENCH
Scope
Sources
Objects
Protocol Instances
Untitled 1
Name
Value
a[3:0]
6
b[3:0]
2
s[3:0]
8
c_out
0
expec...[4:0]
08
expec...[3:0]
8
expected_c
0
error
0
987.981 ns
970.000 ns
975.000 ns
980.000 ns
985.000 ns
990.000 ns
995.000 ns
1,000.0

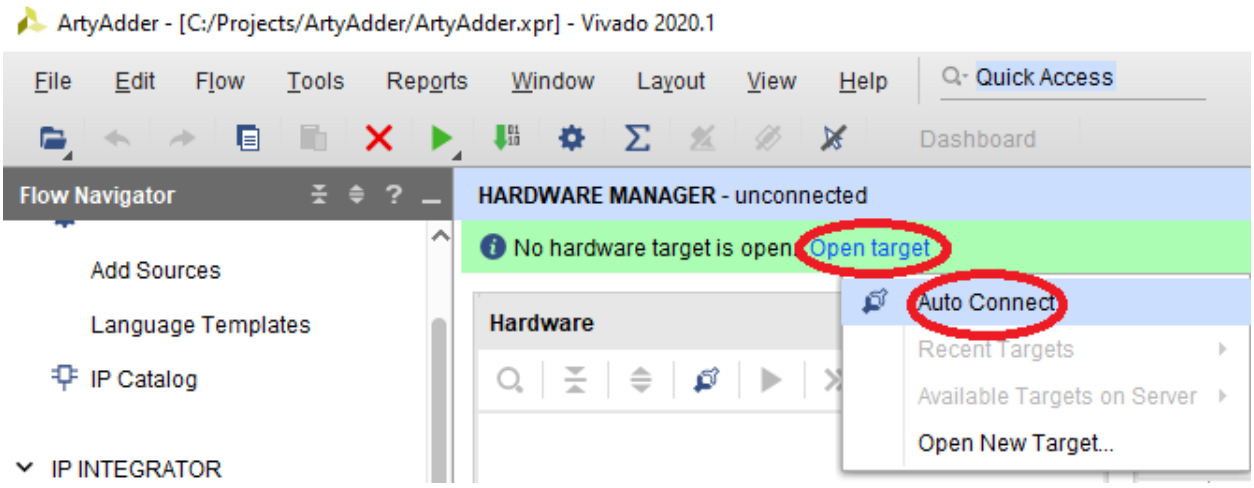

PROJECT MANAGER - ArtyAdder
Sources
Source File Properties
Project Summary
Arty-A7-100.xdc
C:/Projects/ArtyAdder/ArtyAdder.srcs/constrs_1/new/Arty-A7-100.xdc
Switches
set_property -dict { PACKAGE_PIN A8 IOSTANDARD LVCMOS33 } [get_ports { sw[0] }]; #IO_L12N_T1_MRCC_16 Sch=sw[0]
set_property -dict { PACKAGE_PIN C11 IOSTANDARD LVCMOS33 } [get_ports { sw[1] }]; #IO_L13P_T2_MRCC_16 Sch=sw[1]
set_property -dict { PACKAGE_PIN C10 IOSTANDARD LVCMOS33 } [get_ports { sw[2] }]; #IO_L13N_T2_MRCC_16 Sch=sw[2]
set_property -dict { PACKAGE_PIN A10 IOSTANDARD LVCMOS33 } [get_ports { sw[3] }]; #IO_L14P_T2_SRCC_16 Sch=sw[3]
RGB LEDs
#set_property -dict { PACKAGE_PIN E1 IOSTANDARD LVCMOS33 } [get_ports { led0_b }]; #IO_L18N_T2_35 Sch=led0_b
set_property -dict { PACKAGE_PIN F6 IOSTANDARD LVCMOS33 } [get_ports { led0_g }]; #IO_L19N_T3_VREF_35 Sch=led0_g
#set_property -dict { PACKAGE_PIN G6 IOSTANDARD LVCMOS33 } [get_ports { led0_r }]; #IO_L19P_T3_35 Sch=led0_r
#set_property -dict { PACKAGE_PIN G4 IOSTANDARD LVCMOS33 } [get_ports { led1_b }]; #IO_L20P_T3_35 Sch=led1_b
#set_property -dict { PACKAGE_PIN J4 IOSTANDARD LVCMOS33 } [get_ports { led1_g }]; #IO_L21P_T3_DQS_35 Sch=led1_g
#set_property -dict { PACKAGE_PIN G3 IOSTANDARD LVCMOS33 } [get_ports { led1_r }]; #IO_L20N_T3_35 Sch=led1_r
#set_property -dict { PACKAGE_PIN H4 IOSTANDARD LVCMOS33 } [get_ports { led2_b }]; #IO_L21N_T3_DQS_35 Sch=led2_b
#set_property -dict { PACKAGE_PIN J2 IOSTANDARD LVCMOS33 } [get_ports { led2_g }]; #IO_L22N_T3_35 Sch=led2_g
#set_property -dict { PACKAGE_PIN J3 IOSTANDARD LVCMOS33 } [get_ports { led2_r }]; #IO_L22P_T3_35 Sch=led2_r
#set_property -dict { PACKAGE_PIN K2 IOSTANDARD LVCMOS33 } [get_ports { led3_b }]; #IO_L23P_T3_35 Sch=led3_b
#set_property -dict { PACKAGE_PIN H6 IOSTANDARD LVCMOS33 } [get_ports { led3_g }]; #IO_L24P_T3_35 Sch=led3_g
#set_property -dict { PACKAGE_PIN K1 IOSTANDARD LVCMOS33 } [get_ports { led3_r }]; #IO_L23N_T3_35 Sch=led3_r
LEDs
set_property -dict { PACKAGE_PIN H5 IOSTANDARD LVCMOS33 } [get_ports { led[0] }]; #IO_L24N_T3_35 Sch=led[4]
set_property -dict { PACKAGE_PIN J5 IOSTANDARD LVCMOS33 } [get_ports { led[1] }]; #IO_25_35 Sch=led[5]
set_property -dict { PACKAGE_PIN T9 IOSTANDARD LVCMOS33 } [get_ports { led[2] }]; #IO_L24P_T3_A01_D17_14 Sch=led[6]
set_property -dict { PACKAGE_PIN T10 IOSTANDARD LVCMOS33 } [get_ports { led[3] }]; #IO_L24N_T3_A00_D16_14 Sch=led[7]
Buttons
set_property -dict { PACKAGE_PIN D9 IOSTANDARD LVCMOS33 } [get_ports { btn[0] }]; #IO_L6N_T0_VREF_16 Sch=btn[0]
set_property -dict { PACKAGE_PIN C9 IOSTANDARD LVCMOS33 } [get_ports { btn[1] }]; #IO_L11P_T1_SRCC_16 Sch=btn[1]
set_property -dict { PACKAGE_PIN B9 IOSTANDARD LVCMOS33 } [get_ports { btn[2] }]; #IO_L11N_T1_SRCC_16 Sch=btn[2]
set_property -dict { PACKAGE_PIN B8 IOSTANDARD LVCMOS33 } [get_ports { btn[3] }]; #IO_L12P_T1_MRCC_16 Sch=btn[3]

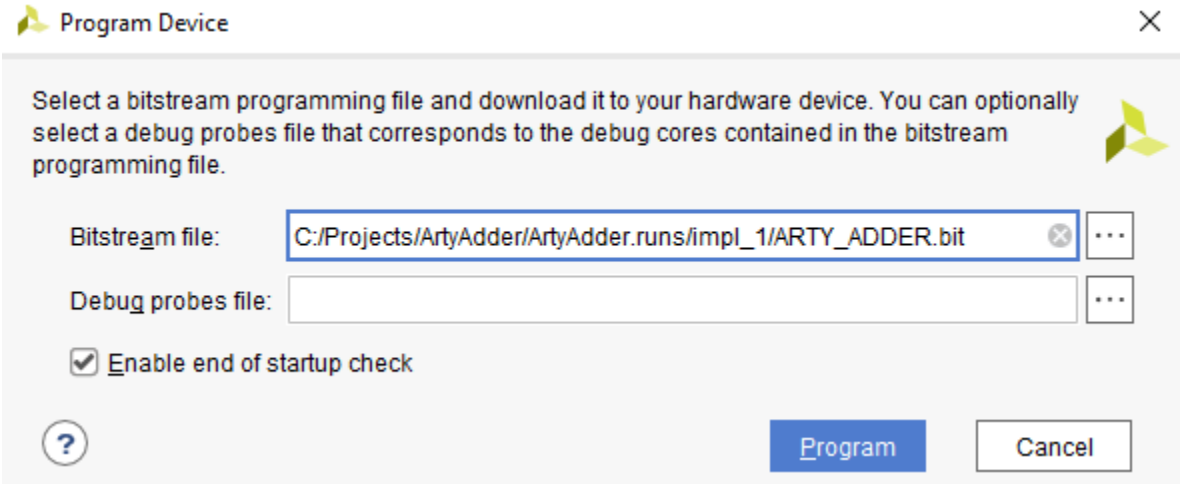

ArtyAdder - [C:/Projects/ArtyAdder/ArtyAdder.xpr] - Vivado 2020.1
File
Edit
Flow
Tools
Reports
Window
Layout
View
Help
Quick Access
Flow Navigator
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
PROJECT MANAGER - ArtyAdder
Sources
Design Sources (1)
ARTY_ADDER(BEHAVIORAL) (ArtyAdder.vhdl) (1)
Constraints (1)
constrs_1 (1)
Arty-A7-35.xdc
Hierarchy
Libraries
Compile Order
Source File Properties
Arty-A7-35.xdc
Enabled
Location:
C:/Projects/ArtyAdder/ArtyAdder.srcs/constrs_1/new
Type:
XDC
General
Properties
Tcl Console
Messages
Log
Reports
Design Runs
Name
Constraints
Status
WNS
TNS
WHS
synth_1
constrs_1
Not started
impl_1
constrs_1
Not started

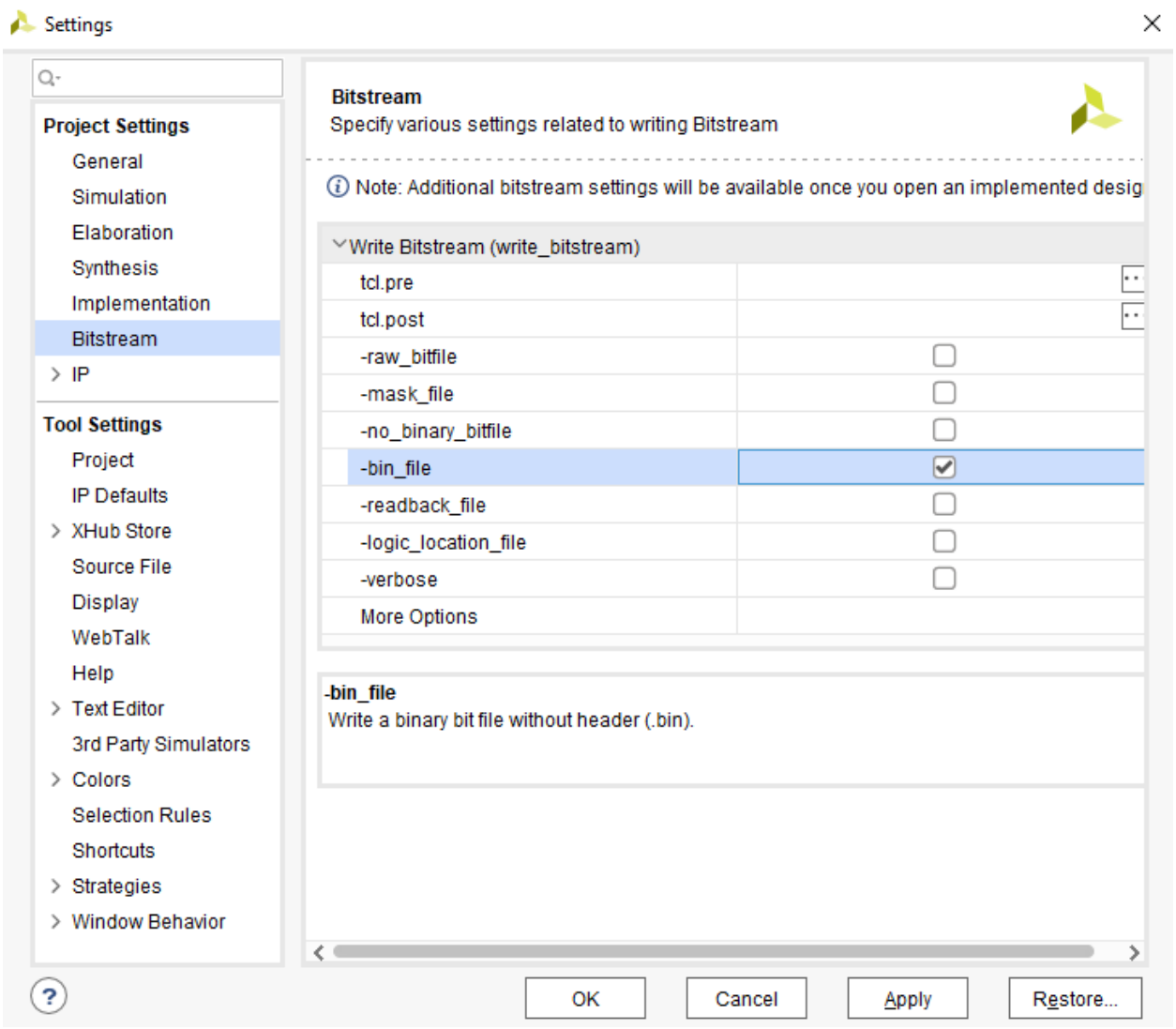

Launch Runs
Launch the selected synthesis or implementation runs.
Launch directory:
<Default Launch Directory>
Options
Launch runs on local host:
Number of jo s:
8
Generate scripts only
Don't show this dialog again
OK
Cancel

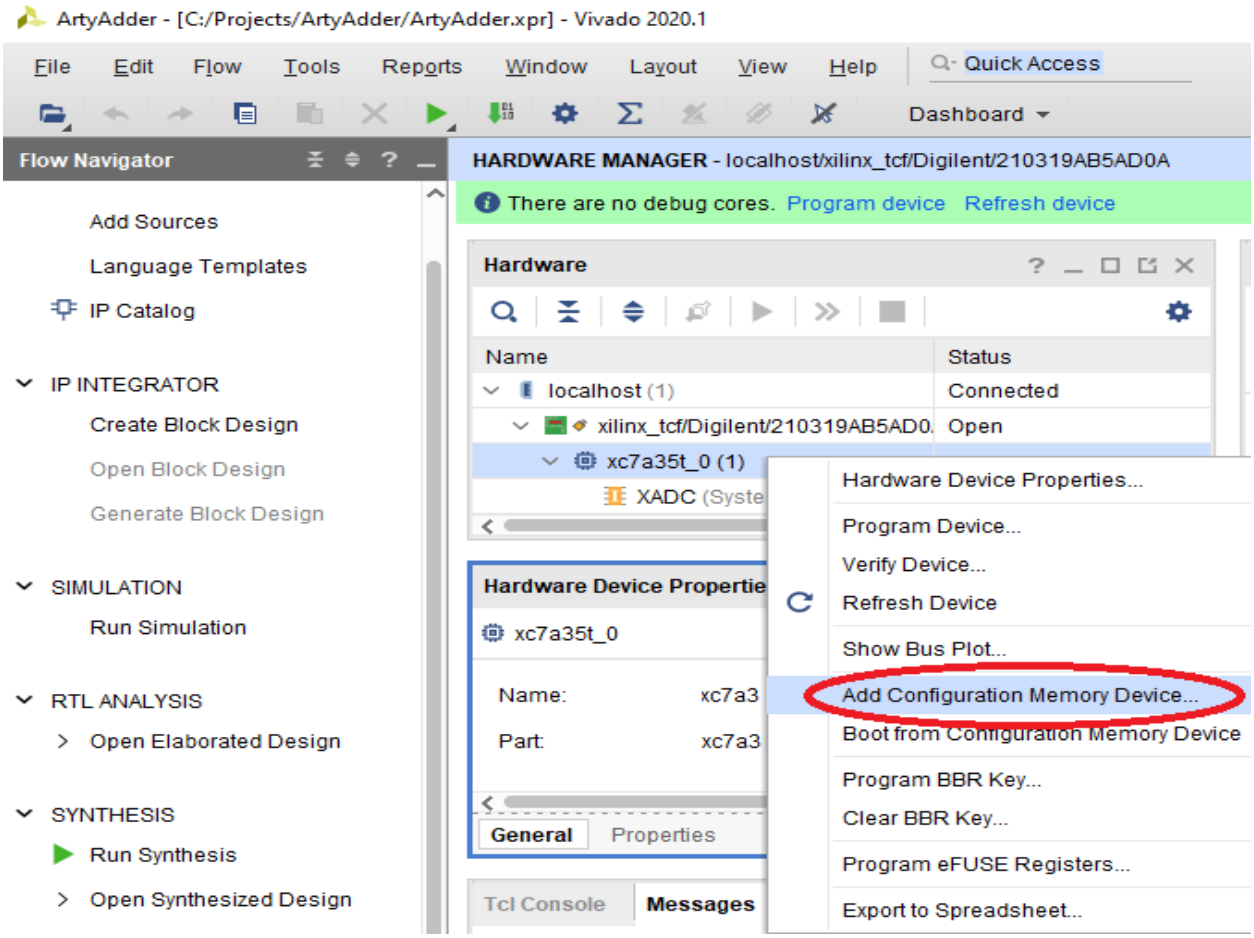

ArtyAdder - [C:/Projects/ArtyAdder/ArtyAdder.xpr] - Vivado 2020.1
File
Edit
Flow
Tools
Reports
Window
Layout
View
Help
Quick Access
Running synth_design
Cancel
Default Layout

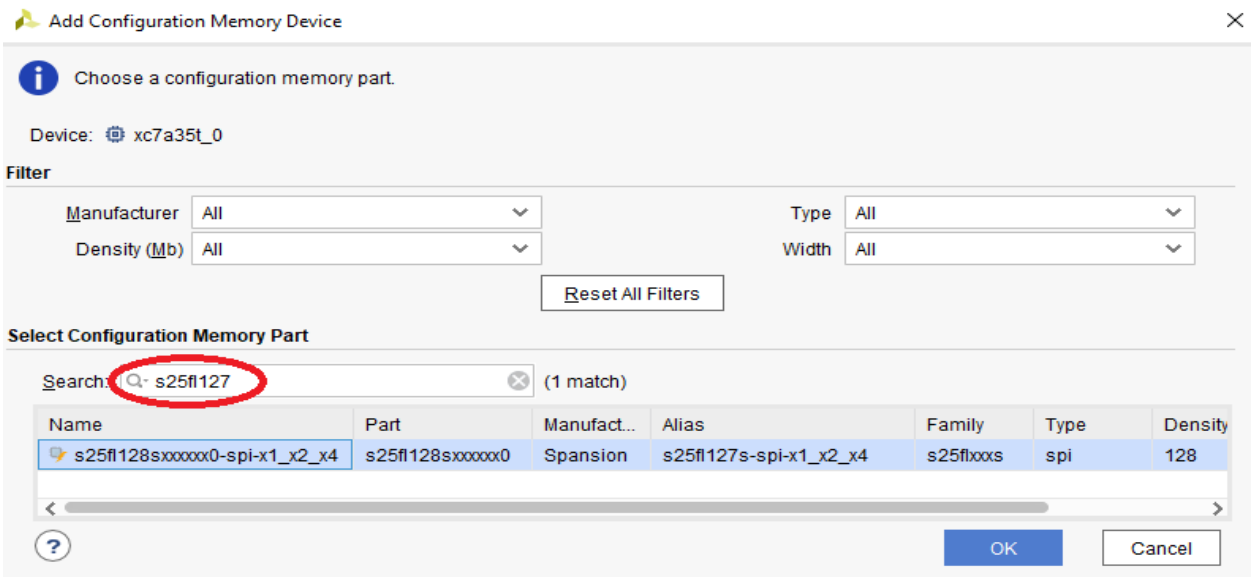

Bitstream Generation Completed
Bitstream Generation successfully completed.
Next
Open Implemented Design
View Reports
Open Hardware Manager
Generate Memory Configuration File
Don't show this dialog again
OK
Cancel

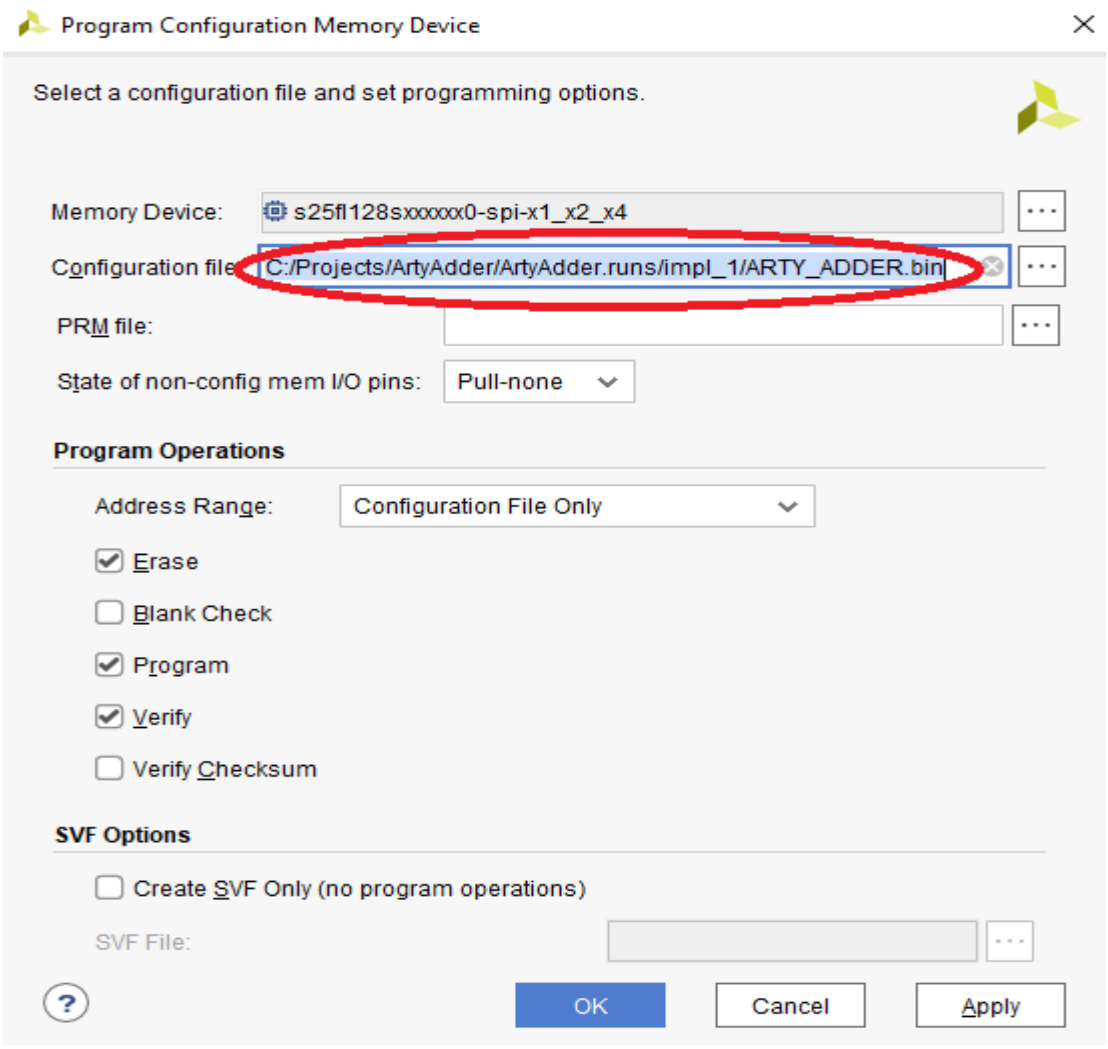

ArtyAdder - [C:/Projects/ArtyAdder/ArtyAdder.xpr] - Vivado 2020.1
File
Edit
Flow
Tools
Reports
Window
Layout
View
Help
Quick Access
Dashboard
Flow Navigator
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
HARDWARE MANAGER - unconnected
No hardware target is open
Open target
Hardware
Auto Connect
Recent Targets
Available Targets on Server
Open New Target...

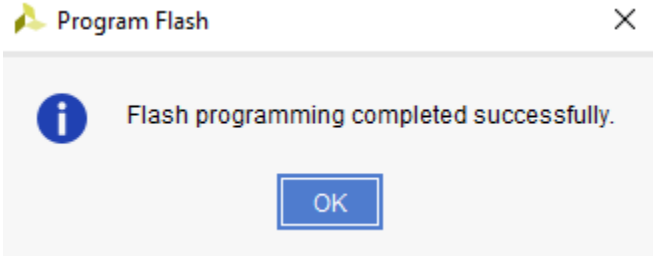

Program Device
Select a bitstream programming file and download it to your hardware device. You can optionally select a debug probes file that corresponds to the debug cores contained in the bitstream programming file.
Bitstream file:
C:/Projects/ArtyAdder/ArtyAdder.runs/impl_1/ARTY_ADDER.bit
Debug probes file:
Enable end of startup check
Program
Cancel


Settings
Project Settings
General
Simulation
Elaboration
Synthesis
Implementation
Bitstream
IP
Tool Settings
Project
IP Defaults
XHub Store
Source File
Display
WebTalk
Help
Text Editor
3rd Party Simulators
Colors
Selection Rules
Shortcuts
Strategies
Window Behavior
Bitstream
Specify various settings related to writing Bitstream
Note: Additional bitstream settings will be available once you open an implemented desig
Write Bitstream (write_bitstream)
tcl.pre
tcl.post
-raw_bitfile
-mask_file
-no_binary_bitfile
-bin_file
-readback_file
-logic_location_file
-verbose
More Options
-bin_file
Write a binary bit file without header (.bin).
OK
Cancel
Apply
Restore...

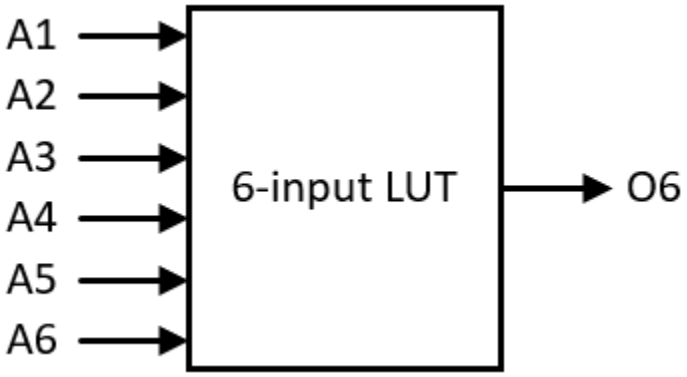

ArtyAdder - [C:/Projects/ArtyAdder/ArtyAdder.xpr] - Vivado 2020.1
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Dashboard
Flow Navigator
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
HARDWARE MANAGER - localhost/xilinx_tcf/Digilent/210319AB5AD0A
There are no debug cores. Program device Refresh device
Hardware
Name
Status
localhost (1)
Connected
xilinx_tcf/Digilent/210319AB5AD0
Open
xc7a35t_0 (1)
XADC (Syste
Hardware Device Properties...
Program Device...
Verify Device...
Refresh Device
Show Bus Plot...
Add Configuration Memory Device...
Boot from Configuration Memory Device
Program BBR Key...
Clear BBR Key...
Program eFUSE Registers...
Export to Spreadsheet...
Hardware Device Propertie
xc7a35t_0
Name: xc7a3
Part: xc7a3
General
Properties
Tcl Console
Messages

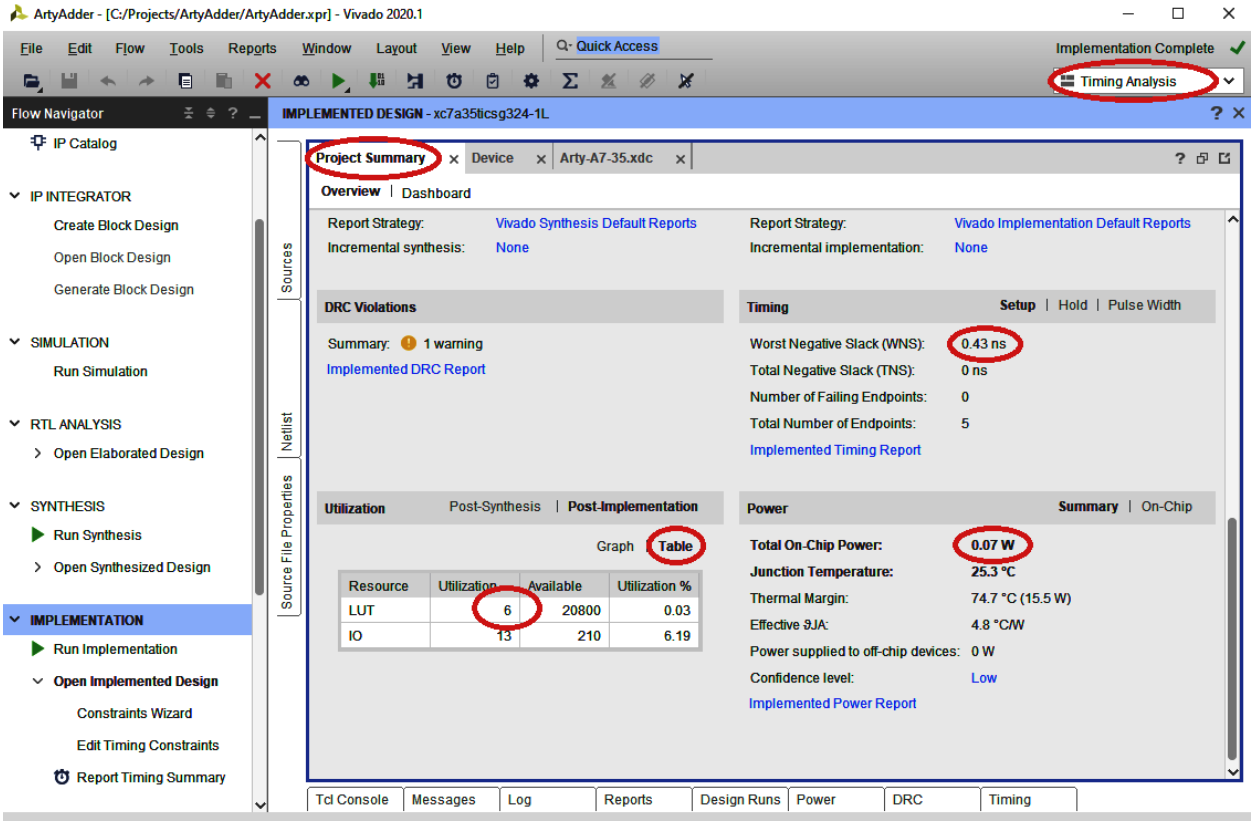

Add Configuration Memory Device
Choose a configuration memory part.
Device: xc7a35t_0
Filter
Manufacturer All
Density (Mb) All
Type All
Width All
Reset All Filters
Select Configuration Memory Part
Search: s25fl127
(1 match)
Name
Part
Manufact...
Alias
Family
Type
Density
s25fl128sxxxxxx0-spi-x1_x2_x4
s25fl128sxxxxxx0
Spansion
s25fl127s-spi-x1_x2_x4
s25flxxxs
spi
128
OK
Cancel

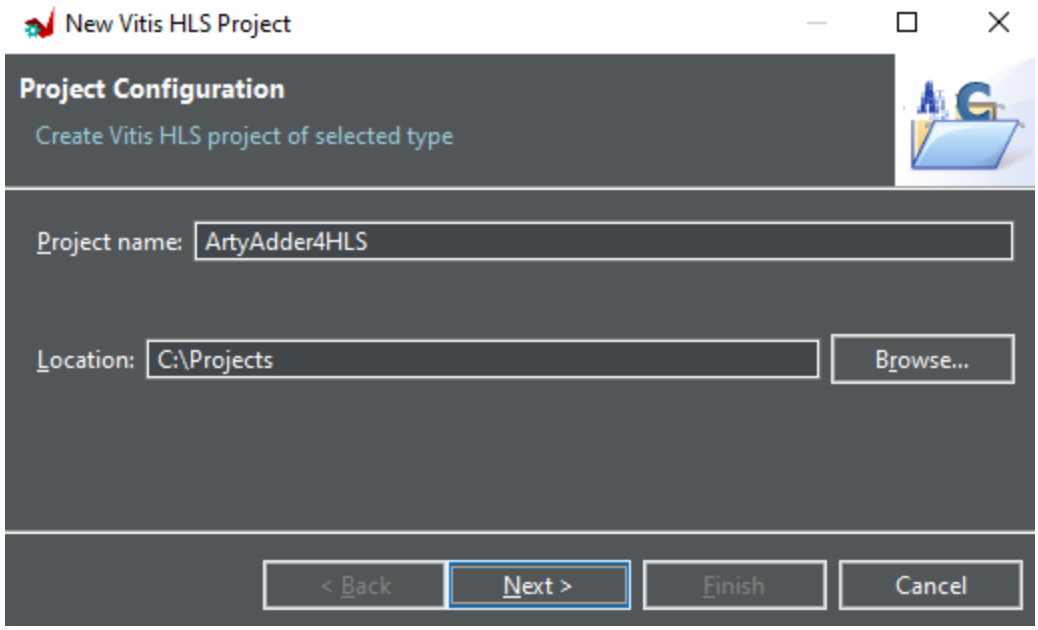

Program Configuration Memory Device
Select a configuration file and set programming options.
Memory Device:
s25fl128sxxxxxx0-spi-x1_x2_x4
Configuration file:
C:/Projects/ArtyAdder/ArtyAdder.runs/impl_1/ARTY_ADDER.bin
PRM file:
State of non-config mem I/O pins:
Pull-none
Program Operations
Address Range:
Configuration File Only
Erase
Blank Check
Program
Verify
Verify Checksum
SVF Options
Create SVF Only (no program operations)
SVF File:
OK
Cancel
Apply

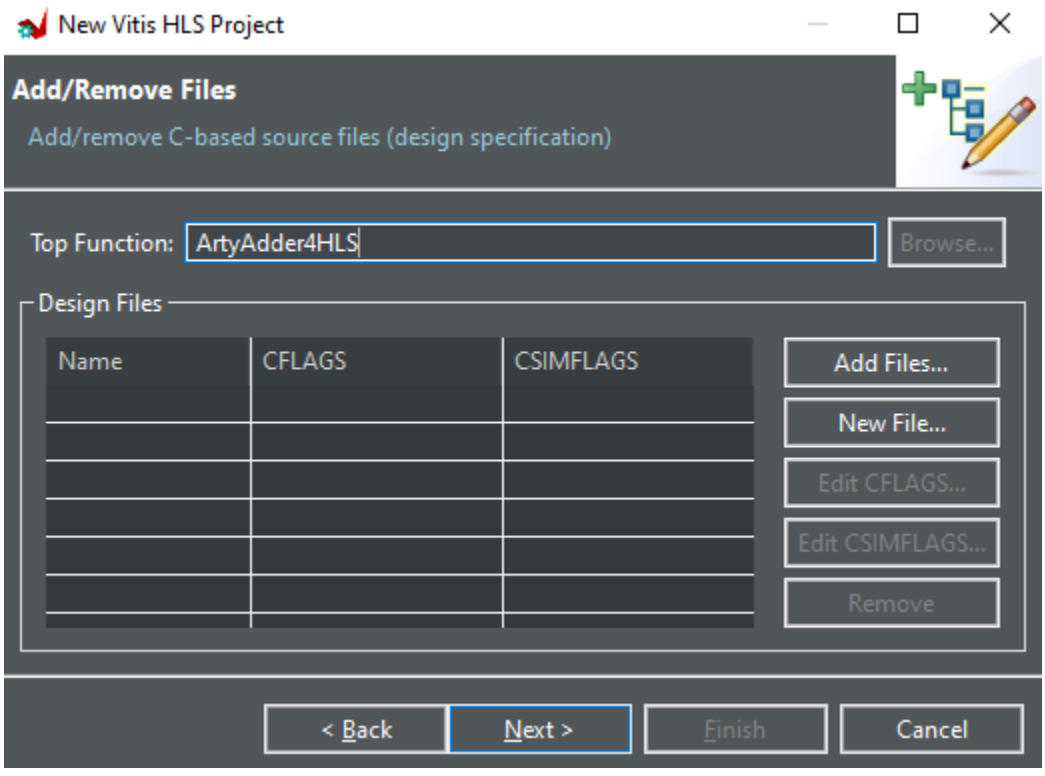

Program Flash
Flash programming completed successfully.
OK

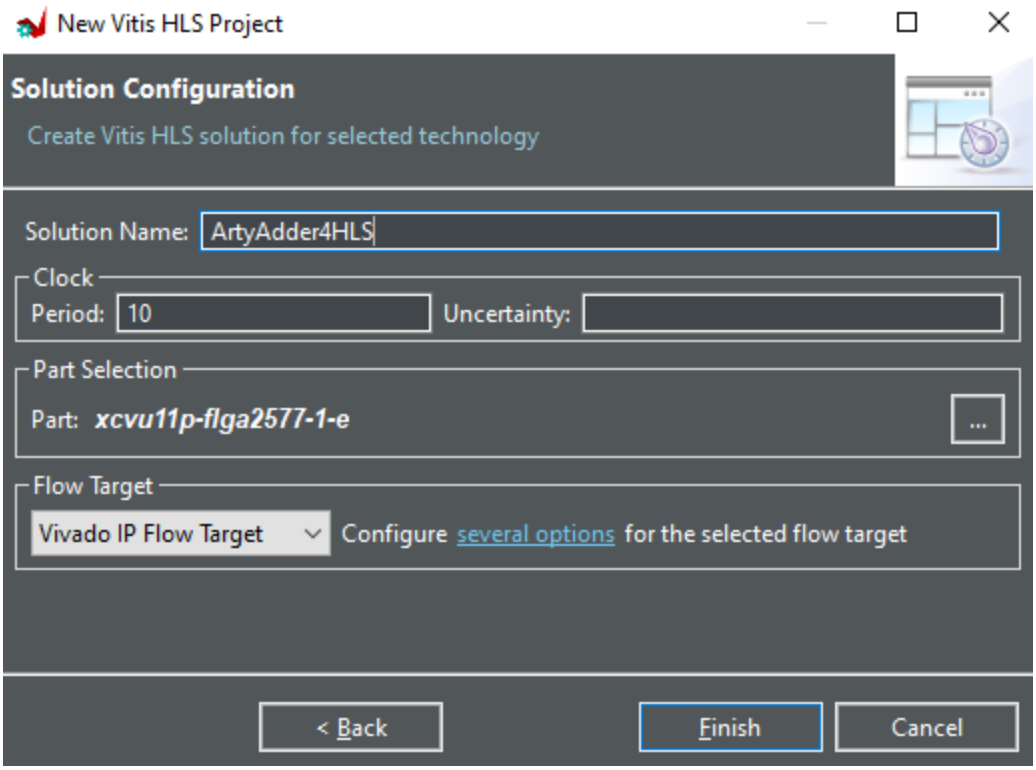
Chapter 5: Implementing systems with FPGAs

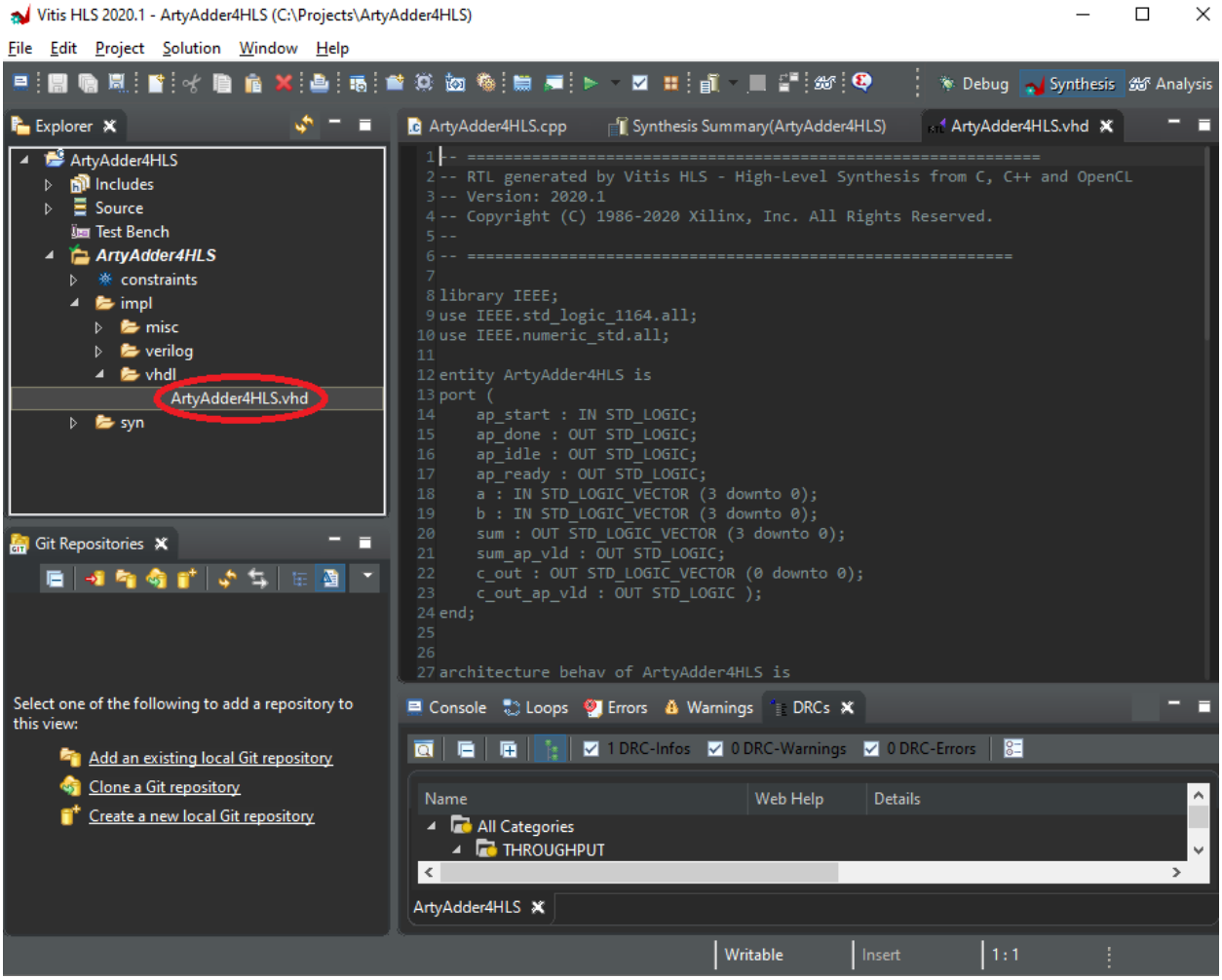


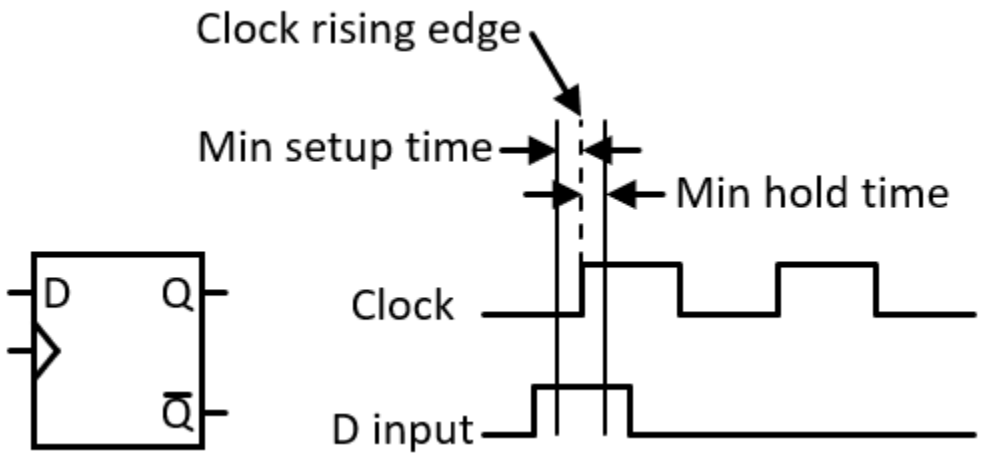


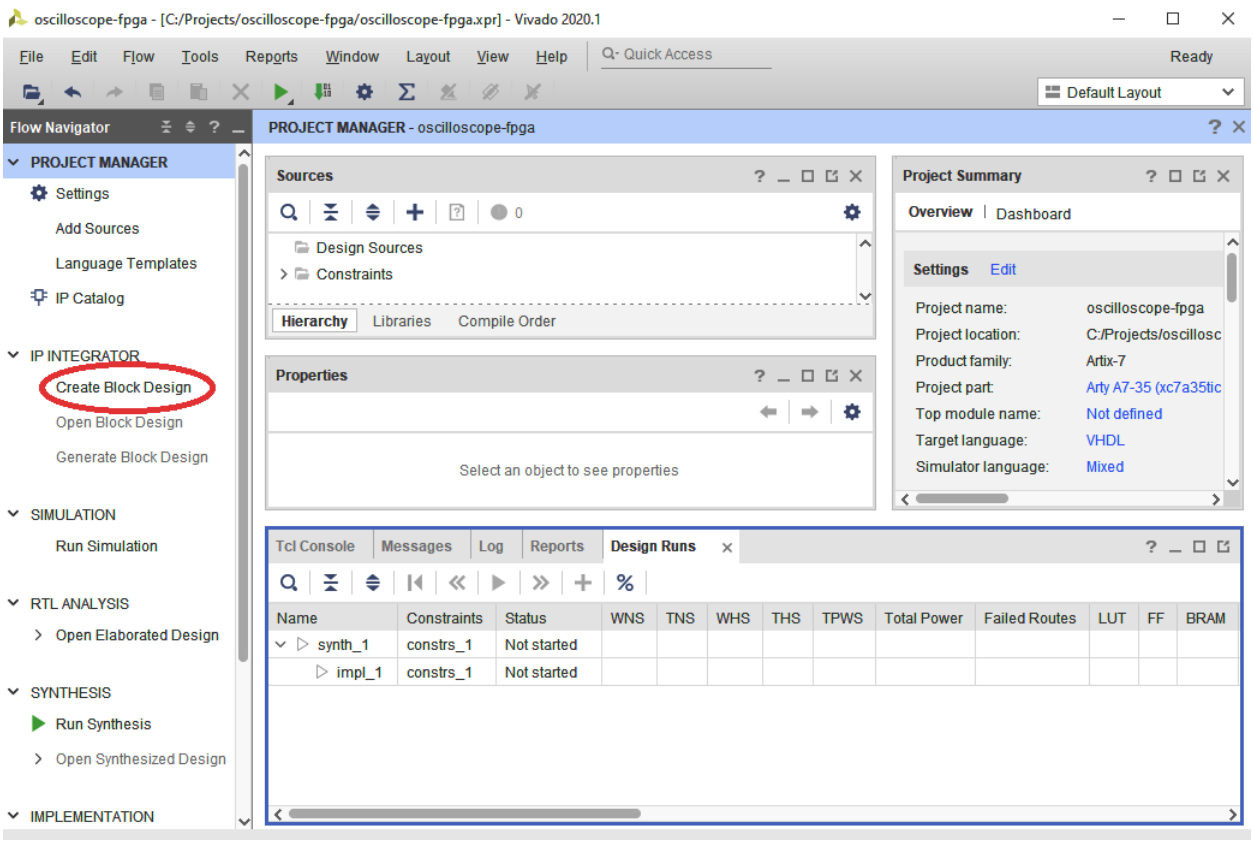

New Vitis HLS Project
Project Configuration
Create Vitis HLS project of selected type
Project name: ArtyAdder4HLS
Location: C:\Projects
Browse...
< Back
Next >
Finish
Cancel

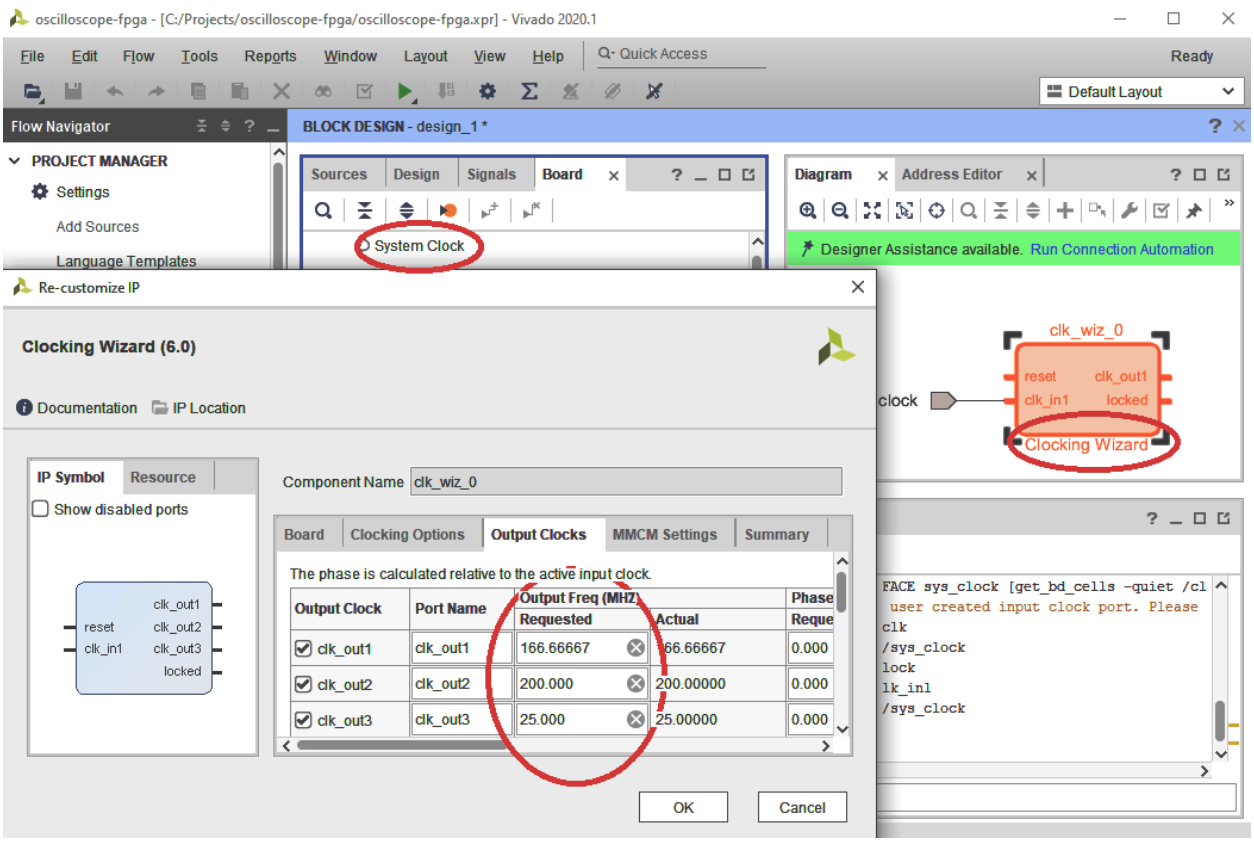

New Vitis HLS Project
Add/Remove Files
Add/remove C-based source files (design specification)
Top Function: ArtyAdder4HLS
Browse...
Design Files
Name
CFLAGS
CSIMFLAGS
Add Files...
New File...
Edit CFLAGS...
Edit CSIMFLAGS...
Remove
< Back
Next >
Finish
Cancel

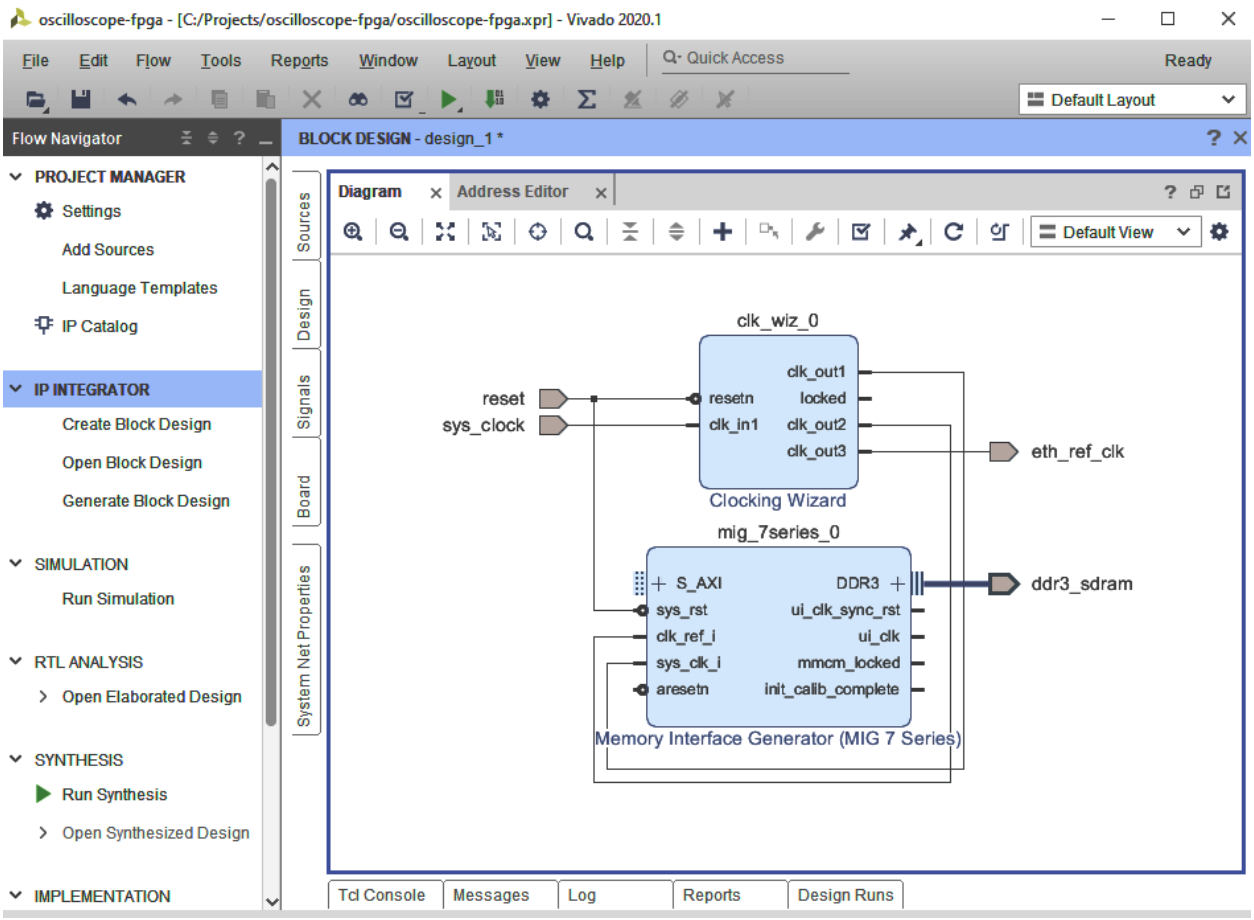

New Vitis HLS Project
Solution Configuration
Create Vitis HLS solution for selected technology
Solution Name:
ArtyAdder4HLS
Clock
Period:
10
Uncertainty:
Part Selection
Part:
xcvu11p-flga2577-1-e
...
Flow Target
Vivado IP Flow Target
Configure several options for the selected flow target
< Back
Finish
Cancel

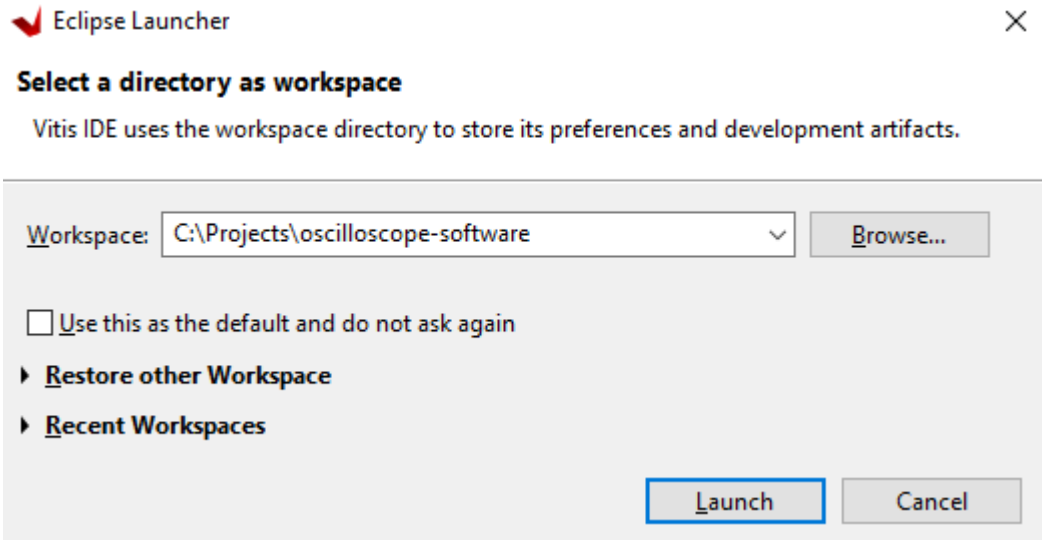

Vitis HLS 2020.1 - ArtyAdder4HLS (C:\Projects\ArtyAdder4HLS)
File Edit Project Solution Window Help
Debug Synthesis Analysis
Explorer
ArtyAdder4HLS
Includes
Source
Test Bench
ArtyAdder4HLS
constraints
impl
misc
verilog
vhdl
ArtyAdder4HLS.vhd
syn
Git Repositories
Select one of the following to add a repository to this view:
Add an existing local Git repository
Clone a Git repository
Create a new local Git repository
ArtyAdder4HLS.cpp
Synthesis Summary(ArtyAdder4HLS)
ArtyAdder4HLS.vhd
-- ==
-- RTL generated by Vitis HLS - High-Level Synthesis from C, C++ and OpenCL
-- Version: 2020.1
-- Copyright (C) 1986-2020 Xilinx, Inc. All Rights Reserved.
--
-- ==
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.numeric_std.all;
entity ArtyAdder4HLS is
port (
ap_start : IN STD_LOGIC;
ap_done : OUT STD_LOGIC;
ap_idle : OUT STD_LOGIC;
ap_ready : OUT STD_LOGIC;
a : IN STD_LOGIC_VECTOR (3 downto 0);
b : IN STD_LOGIC_VECTOR (3 downto 0);
sum : OUT STD_LOGIC_VECTOR (3 downto 0);
sum_ap_vld : OUT STD_LOGIC;
c_out : OUT STD_LOGIC_VECTOR (0 downto 0);
c_out_ap_vld : OUT STD_LOGIC);
end;
architecture behav of ArtyAdder4HLS is
Console Loops Errors Warnings DRCs
1 DRC-Infos 0 DRC-Warnings 0 DRC-Errors
Name Web Help Details
All Categories
THROUGHPUT
ArtyAdder4HLS
Writable Insert 1:1

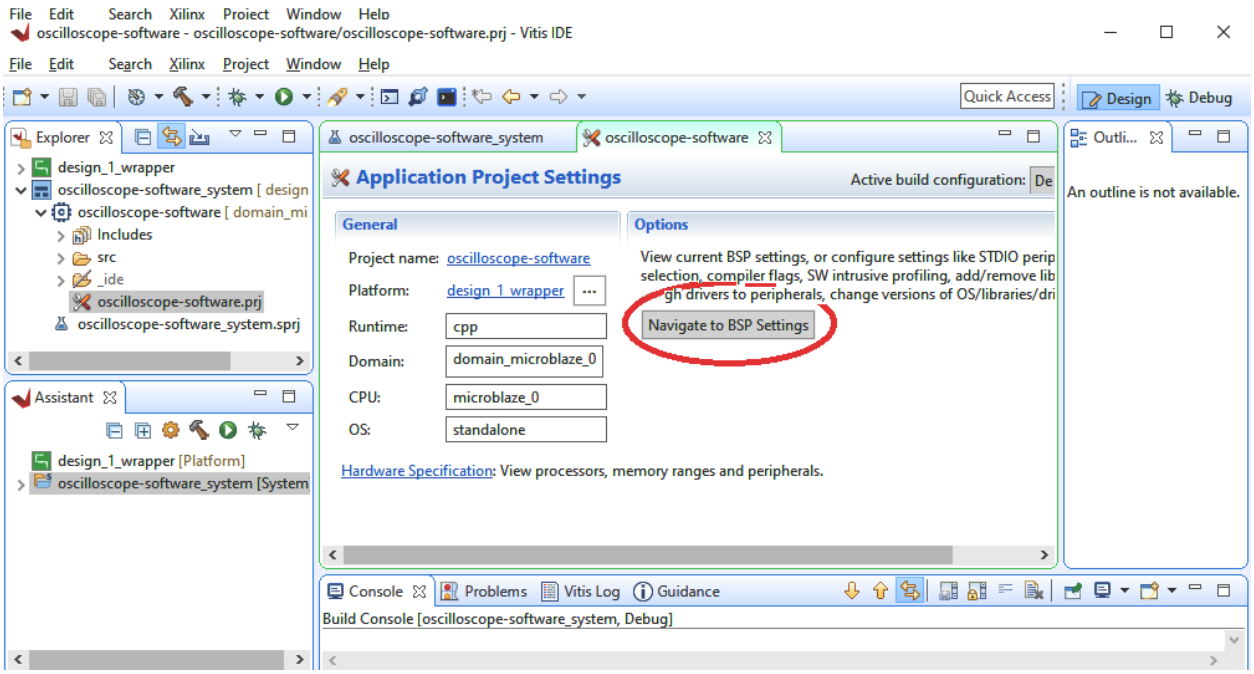

Clock rising edge
Min setup time
Min hold time
D
Q
Q
Clock
D input

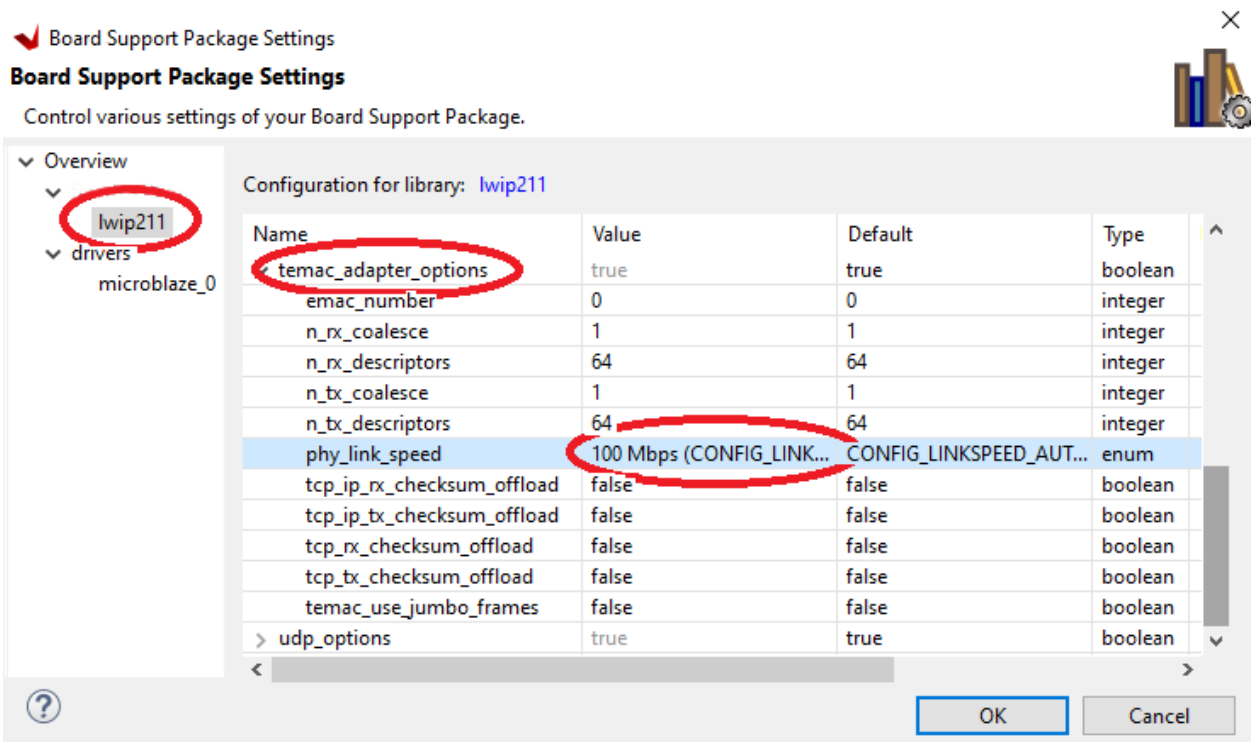

oscilloscope-fpga - [C:/Projects/oscilloscope-fpga/oscilloscope-fpga.xpr] - Vivado 2020.1
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Ready
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
PROJECT MANAGER - oscilloscope-fpga
Sources
Design Sources
Constraints
Hierarchy
Libraries
Compile Order
Properties
Select an object to see properties
Project Summary
Overview
Dashboard
Settings
Edit
Project name: oscilloscope-fpga
Project location: C:/Projects/oscillosc
Product family: Artix-7
Project part: Arty A7-35 (xc7a35tic
Top module name: Not defined
Target language: VHDL
Simulator language: Mixed
Tcl Console
Messages
Log
Reports
Design Runs
Name
Constraints
Status
WNS
TNS
WHS
THS
TPWS
Total Power
Failed Routes
LUT
FF
BRAM
synth_1
constrs_1
Not started
impl_1
constrs_1
Not started

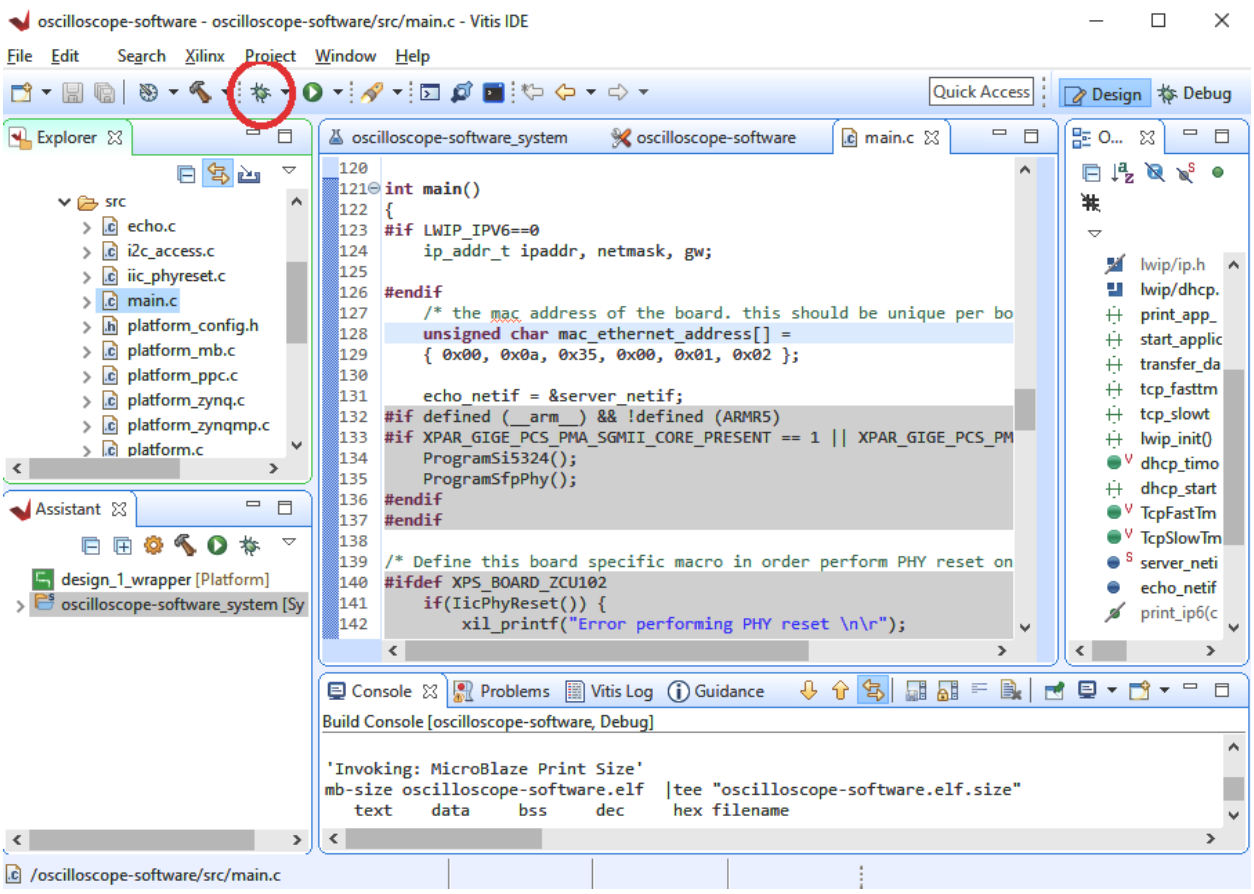

oscilloscope-fpga - [C:/Projects/oscilloscope-fpga/oscilloscope-fpga.xpr] - Vivado 2020.1
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Ready
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
BLOCK DESIGN - design_1 *
Sources Design Signals Board
System Clock
Diagram Address Editor
Designer Assistance available. Run Connection Automation
clk_wiz_0
reset clk_out1
clk_in1 locked
Clocking Wizard
clock
Re-customize IP
Clocking Wizard (6.0)
Documentation IP Location
IP Symbol Resource
Show disabled ports
clk_out1
reset clk_out2
clk_in1 clk_out3
locked
Component Name clk_wiz_0
Board Clocking Options Output Clocks MMCM Settings Summary
The phase is calculated relative to the active input clock.
Output Clock Port Name Output Freq (MHz) Requested Actual Phase Reque
clk_out1 clk_out1 166.66667 166.66667 0.000
clk_out2 clk_out2 200.000 200.00000 0.000
clk_out3 clk_out3 25.000 25.00000 0.000
OK Cancel
FACE sys_clock [get_bd_cells -quiet /cl
user created input clock port. Please
clk
/sys_clock
lock
lk_in1
/sys_clock

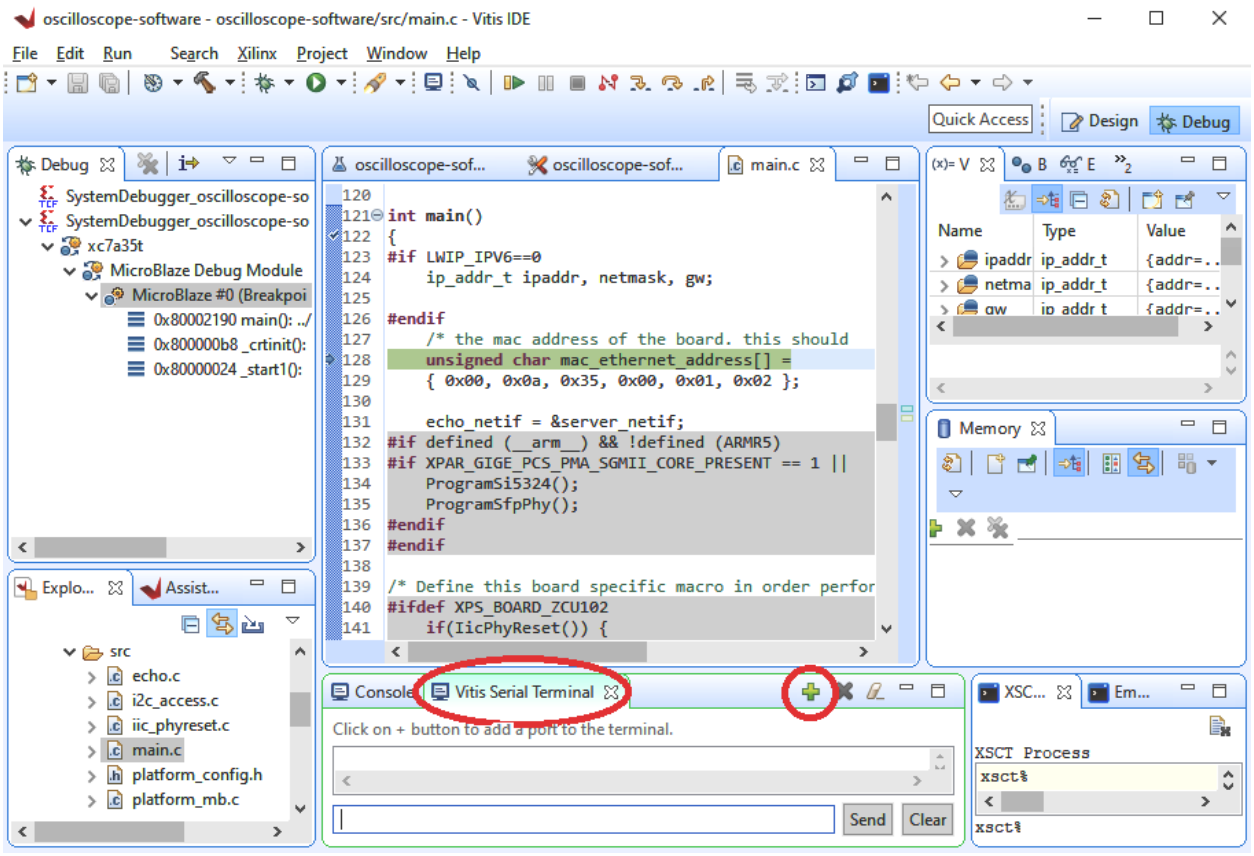

oscilloscope-fpga - [C:/Projects/oscilloscope-fpga/oscilloscope-fpga.xpr] - Vivado 2020.1
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Ready
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
BLOCK DESIGN - design_1 *
Sources
Design
Signals
Board
System Net Properties
Diagram
Address Editor
Default View
clk_wiz_0
reset
sys_clock
resetn
clk_in1
clk_out1
locked
clk_out2
clk_out3
eth_ref_clk
Clocking Wizard
mig_7series_0
S_AXI
sys_rst
clk_ref_i
sys_clk_i
aresetn
DDR3
ui_clk_sync_rst
ui_clk
mmcm_locked
init_calib_complete
ddr3_sdram
Memory Interface Generator (MIG 7 Series)
Tcl Console
Messages
Log
Reports
Design Runs

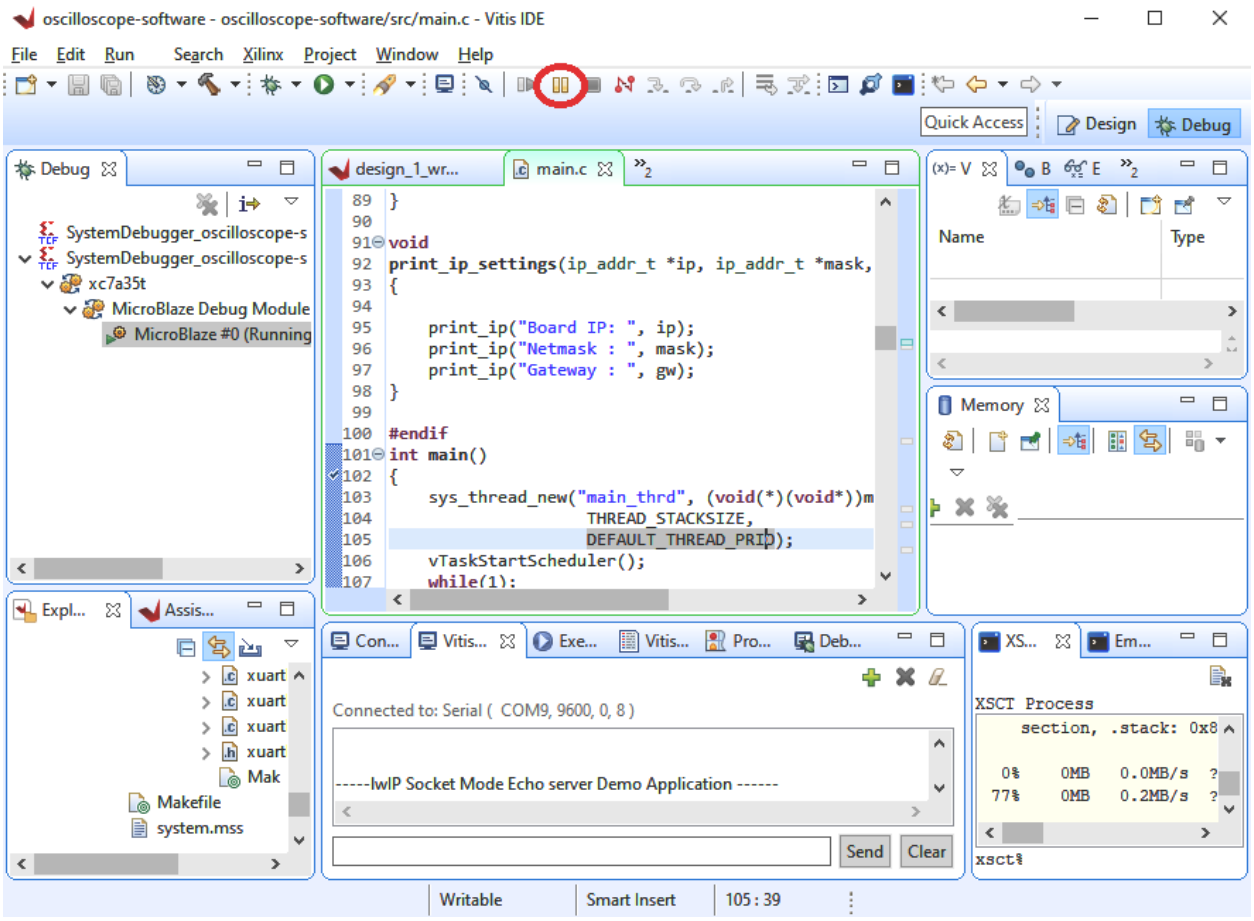

Eclipse Launcher
Select a directory as workspace
Vitis IDE uses the workspace directory to store its preferences and development artifacts.
Workspace:
C:\Projects\oscilloscope-software
Browse...
Use this as the default and do not ask again
Restore other Workspace
Recent Workspaces
Launch
Cancel


File Edit Search Xilinx Project Window Help
oscilloscope-software - oscilloscope-software/oscilloscope-software.prj - Vitis IDE
Quick Access
Design
Debug
Explorer
design_1_wrapper
oscilloscope-software_system [design
oscilloscope-software [domain_mi
Includes
src
_ide
oscilloscope-software.prj
oscilloscope-software_system.sprj
Assistant
design_1_wrapper [Platform]
oscilloscope-software_system [System
oscilloscope-software_system
oscilloscope-software
Application Project Settings
Active build configuration:
General
Options
Project name: oscilloscope-software
Platform: design_1_wrapper
Runtime: cpp
Domain: domain_microblaze_0
CPU: microblaze_0
OS: standalone
View current BSP settings, or configure settings like STDIO perip
selection, compiler flags, SW intrusive profiling, add/remove lib
gh drivers to peripherals, change versions of OS/libraries/dri
Navigate to BSP Settings
Hardware Specification: View processors, memory ranges and peripherals.
Outli...
An outline is not available.
Console
Problems
Vitis Log
Guidance
Build Console [oscilloscope-software_system, Debug]

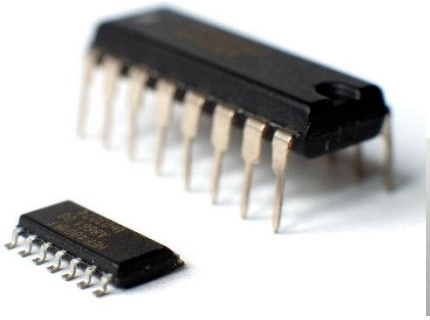

Board Support Package Settings
Board Support Package Settings
Control various settings of your Board Support Package.
Overview
lwip211
drivers
microblaze_0
Configuration for library: lwip211
Name
Value
Default
Type
temac_adapter_options
true
true
boolean
emac_number
0
0
integer
n_rx_coalesce
1
1
integer
n_rx_descriptors
64
64
integer
n_tx_coalesce
1
1
integer
n_tx_descriptors
64
64
integer
phy_link_speed
100 Mbps (CONFIG_LINK...
CONFIG_LINKSPEED_AUT...
enum
tcp_ip_rx_checksum_offload
false
false
boolean
tcp_ip_tx_checksum_offload
false
false
boolean
tcp_rx_checksum_offload
false
false
boolean
tcp_tx_checksum_offload
false
false
boolean
temac_use_jumbo_frames
false
false
boolean
udp_options
true
true
boolean
OK
Cancel

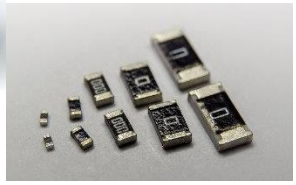

oscilloscope-software - oscilloscope-software/src/main.c - Vitis IDE
File Edit Search Xilinx Project Window Help
Quick Access
Design
Debug
Explorer
src
echo.c
i2c_access.c
iic_phyreset.c
main.c
platform_config.h
platform_mb.c
platform_ppc.c
platform_zynq.c
platform_zynqmp.c
platform.c
Assistant
design_1_wrapper [Platform]
oscilloscope-software_system [Sy
oscilloscope-software_system
oscilloscope-software
main.c
120
121 int main()
122 {
123 #if LWIP_IPV6==0
124 ip_addr_t ipaddr, netmask, gw;
125
126 #endif
127 /* the mac address of the board. this should be unique per bo
128 unsigned char mac_ethernet_address[] =
129 { 0x00, 0x0a, 0x35, 0x00, 0x01, 0x02 };
130
131 echo_netif = &server_netif;
132 #if defined (__arm__) && !defined (ARMR5)
133 #if XPAR_GIGE_PCS_PMA_SGMII_CORE_PRESENT == 1 || XPAR_GIGE_PCS_PM
134 ProgramSi5324();
135 ProgramSfpPhy();
136 #endif
137 #endif
138
139 /* Define this board specific macro in order perform PHY reset on
140 #ifdef XPS_BOARD_ZCU102
141 if(IicPhyReset()) {
142 xil_printf("Error performing PHY reset \n\r");
lwip/ip.h
lwip/dhcp.
print_app_
start_applic
transfer_da
tcp_fasttm
tcp_slowt
lwip_init()
dhcp_timo
dhcp_start
TcpFastTm
TcpSlowTm
server_neti
echo_netif
print_ip6(c
Console
Problems
Vitis Log
Guidance
Build Console [oscilloscope-software, Debug]
'Invoking: MicroBlaze Print Size'
mb-size oscilloscope-software.elf |tee "oscilloscope-software.elf.size"
text data bss dec hex filename
/oscilloscope-software/src/main.c

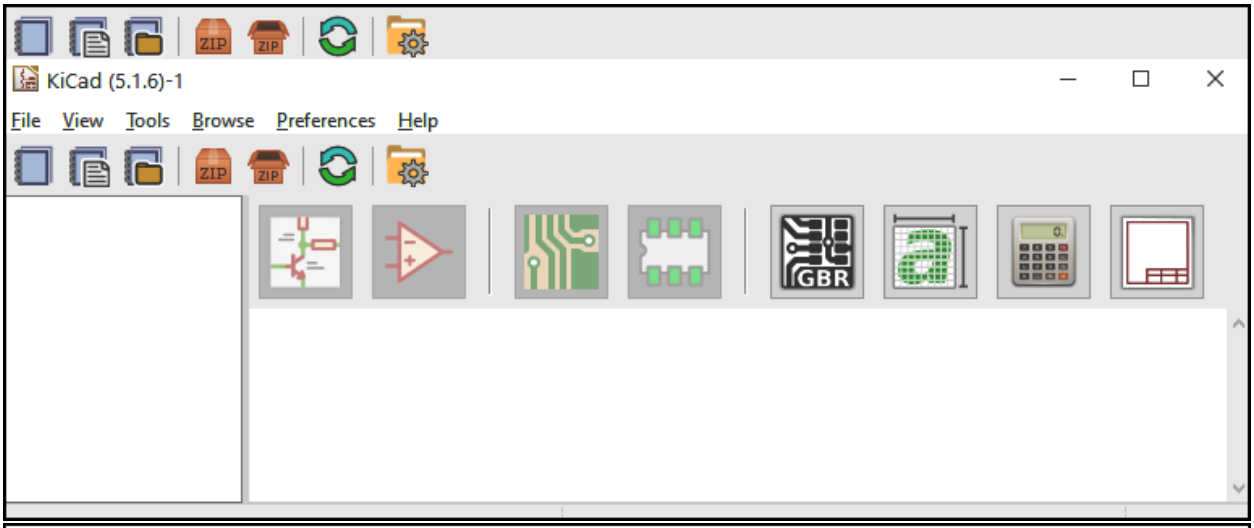

oscilloscope-software - oscilloscope-software/src/main.c - Vitis IDE
File Edit Run Search Xilinx Project Window Help
Quick Access
Design
Debug
Debug
SystemDebugger_oscilloscope-so
SystemDebugger_oscilloscope-so
xc7a35t
MicroBlaze Debug Module
MicroBlaze #0 (Breakpoi
0x80002190 main(): ../
0x800000b8 _crtinit():
0x80000024 _start1():
oscilloscope-sof...
oscilloscope-sof...
main.c
120
121 int main()
122 {
123 #if LWIP_IPV6==0
124 ip_addr_t ipaddr, netmask, gw;
125
126 #endif
127 /* the mac address of the board. this should
128 unsigned char mac_ethernet_address[] =
129 { 0x00, 0x0a, 0x35, 0x00, 0x01, 0x02 };
130
131 echo_netif = &server_netif;
132 #if defined (__arm__) && !defined (ARMR5)
133 #if XPAR_GIGE_PCS_PMA_SGMII_CORE_PRESENT == 1 ||
134 ProgramSi5324();
135 ProgramSfpPhy();
136 #endif
137 #endif
138
139 /* Define this board specific macro in order perfor
140 #ifdef XPS_BOARD_ZCU102
141 if(IicPhyReset()) {
(x)= V
B
E
Name
Type
Value
ipaddr
ip_addr_t
{addr=..
netma
ip_addr_t
{addr=..
gw
ip_addr_t
{addr=..
Memory
Explo...
Assist...
src
echo.c
i2c_access.c
iic_phyreset.c
main.c
platform_config.h
platform_mb.c
Console
Vitis Serial Terminal
Click on + button to add a port to the terminal.
Send
Clear
XSC...
Em...
XSCT Process
xsct%
xsct%

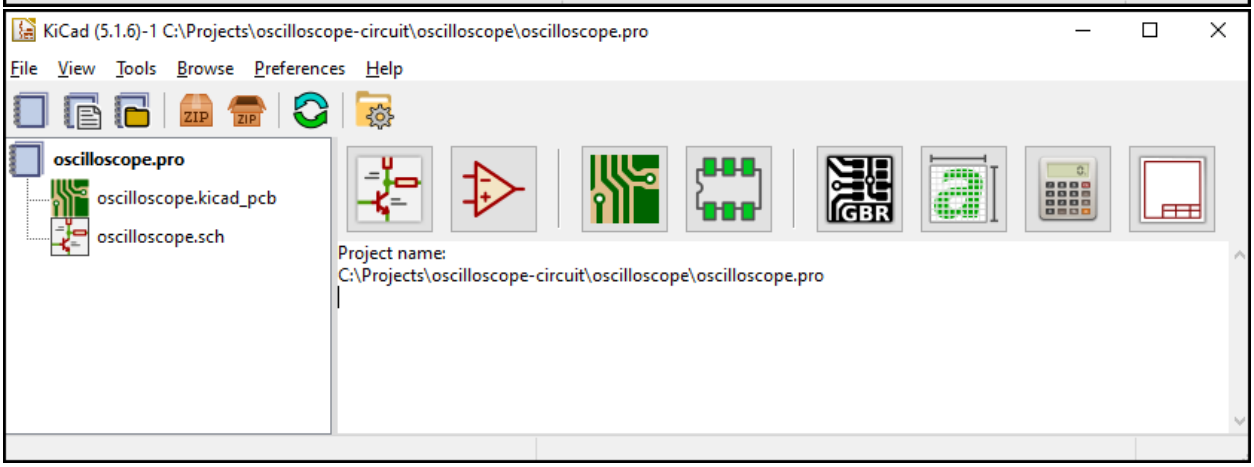

oscilloscope-software - oscilloscope-software/src/main.c - Vitis IDE
File Edit Run Search Xilinx Project Window Help
Quick Access
Design
Debug
Debug
SystemDebugger_oscilloscope-s
SystemDebugger_oscilloscope-s
xc7a35t
MicroBlaze Debug Module
MicroBlaze #0 (Running
design_1_wr...
main.c
89 }
90
91 void
92 print_ip_settings(ip_addr_t *ip, ip_addr_t *mask,
93 {
94
95 print_ip("Board IP: ", ip);
96 print_ip("Netmask : ", mask);
97 print_ip("Gateway : ", gw);
98 }
99
100 #endif
101 int main()
102 {
103 sys_thread_new("main_thrd", (void(*)(void*))m
104 THREAD_STACKSIZE,
105 DEFAULT_THREAD_PRIO);
106 vTaskStartScheduler();
107 while(1);
Name
Type
Memory
Expl...
Assis...
xuart
xuart
xuart
xuart
Mak
Makefile
system.mss
Con...
Vitis...
Exe...
Vitis...
Pro...
Deb...
Connected to: Serial (COM9, 9600, 0, 8)
-----lwIP Socket Mode Echo server Demo Application ------
Send
Clear
XS...
Em...
XSCT Process
section, .stack: 0x8
0% 0MB 0.0MB/s ?
77% 0MB 0.2MB/s ?
xsct%
Writable
Smart Insert
105 : 39

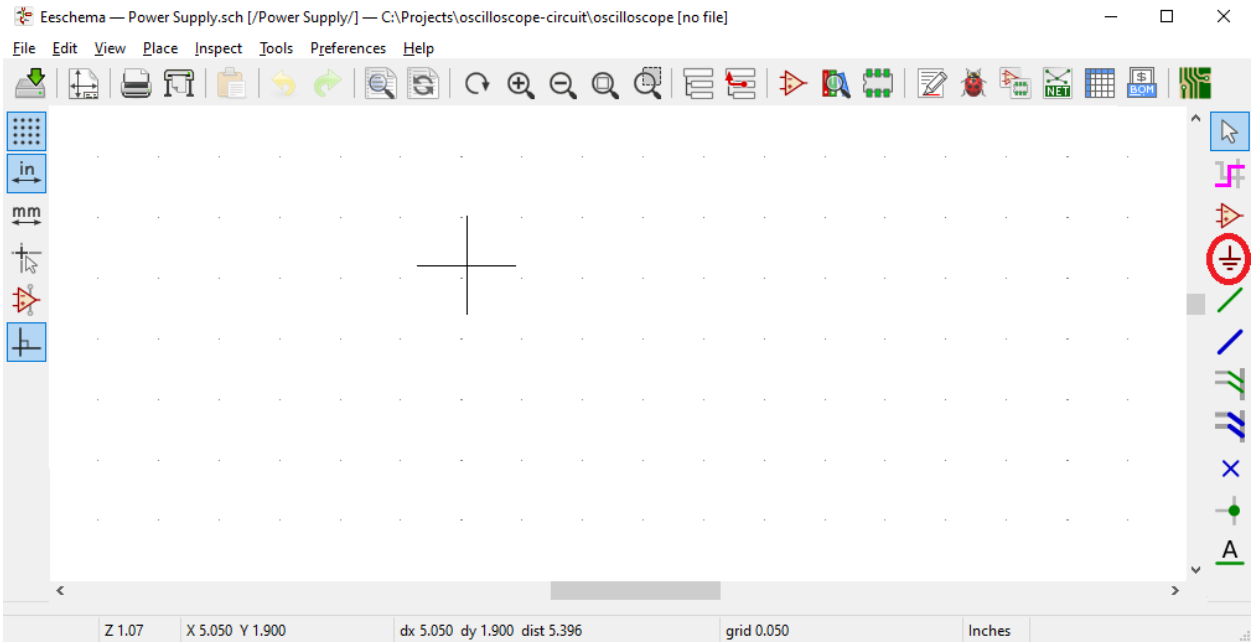
Chapter 6: Designing Circuits with KiCad

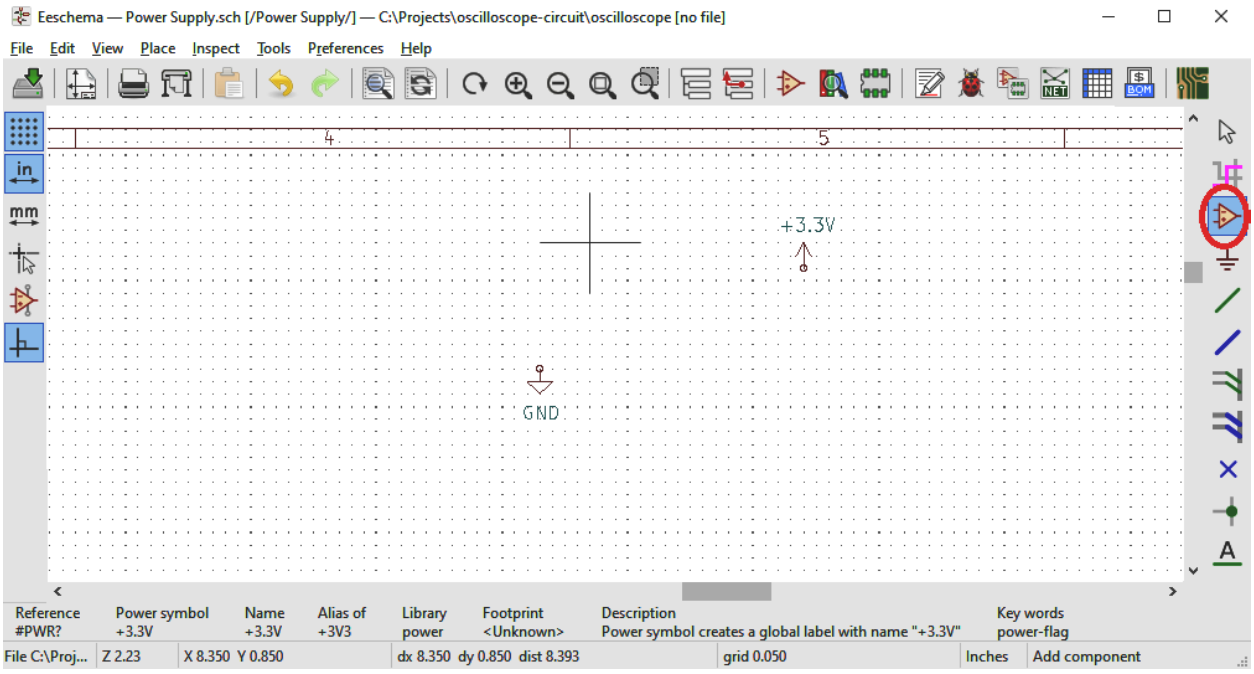


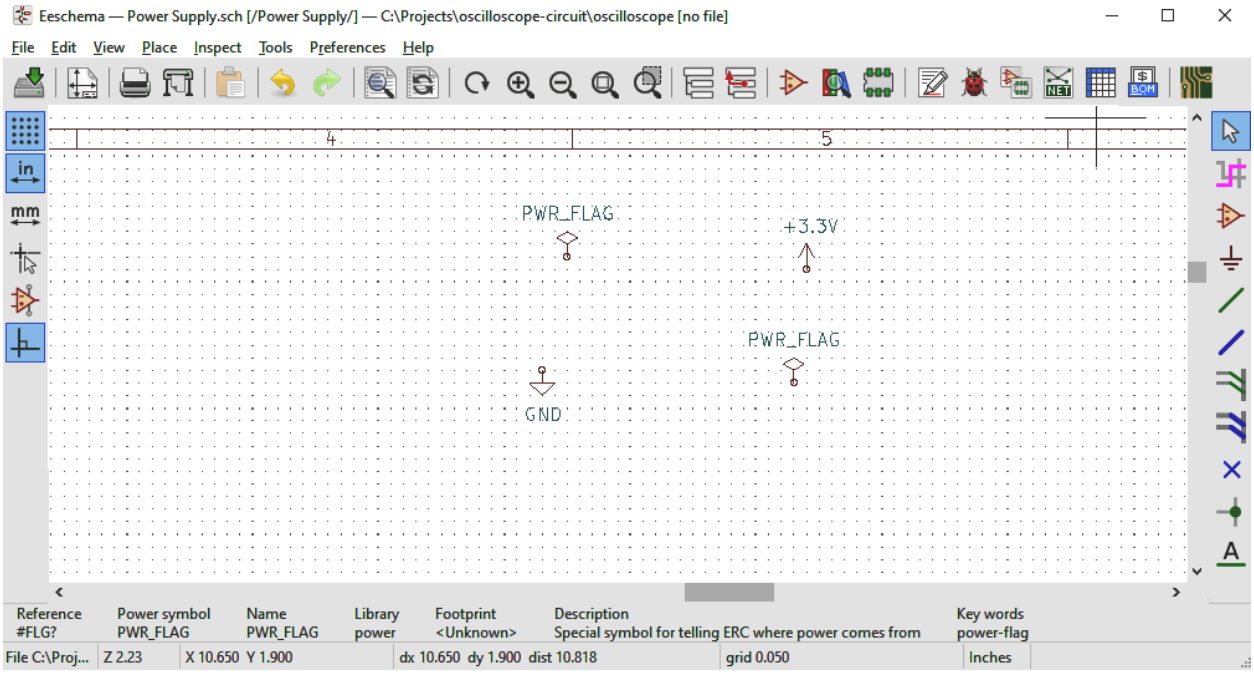


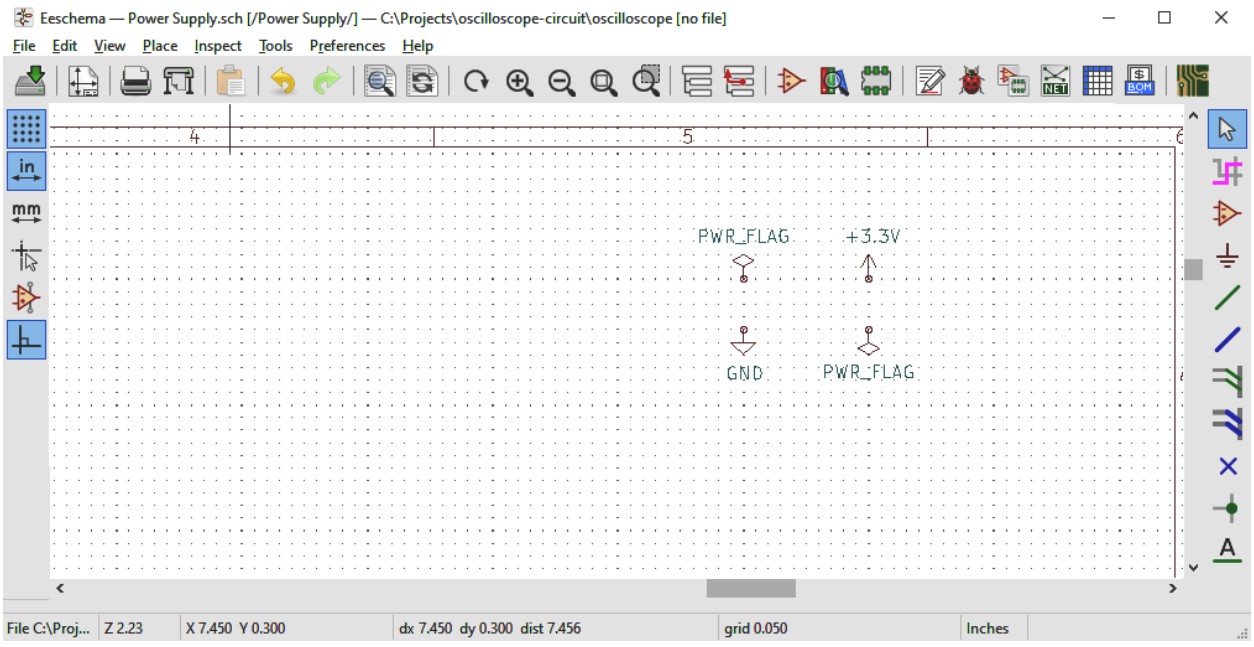


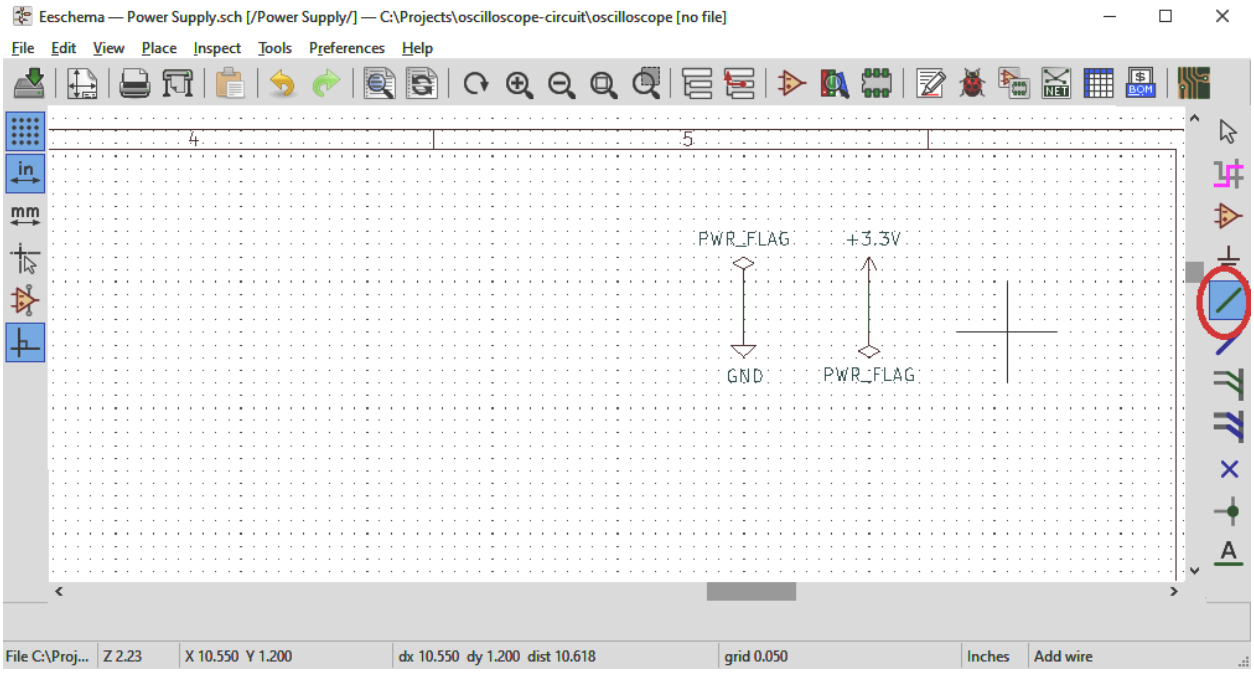


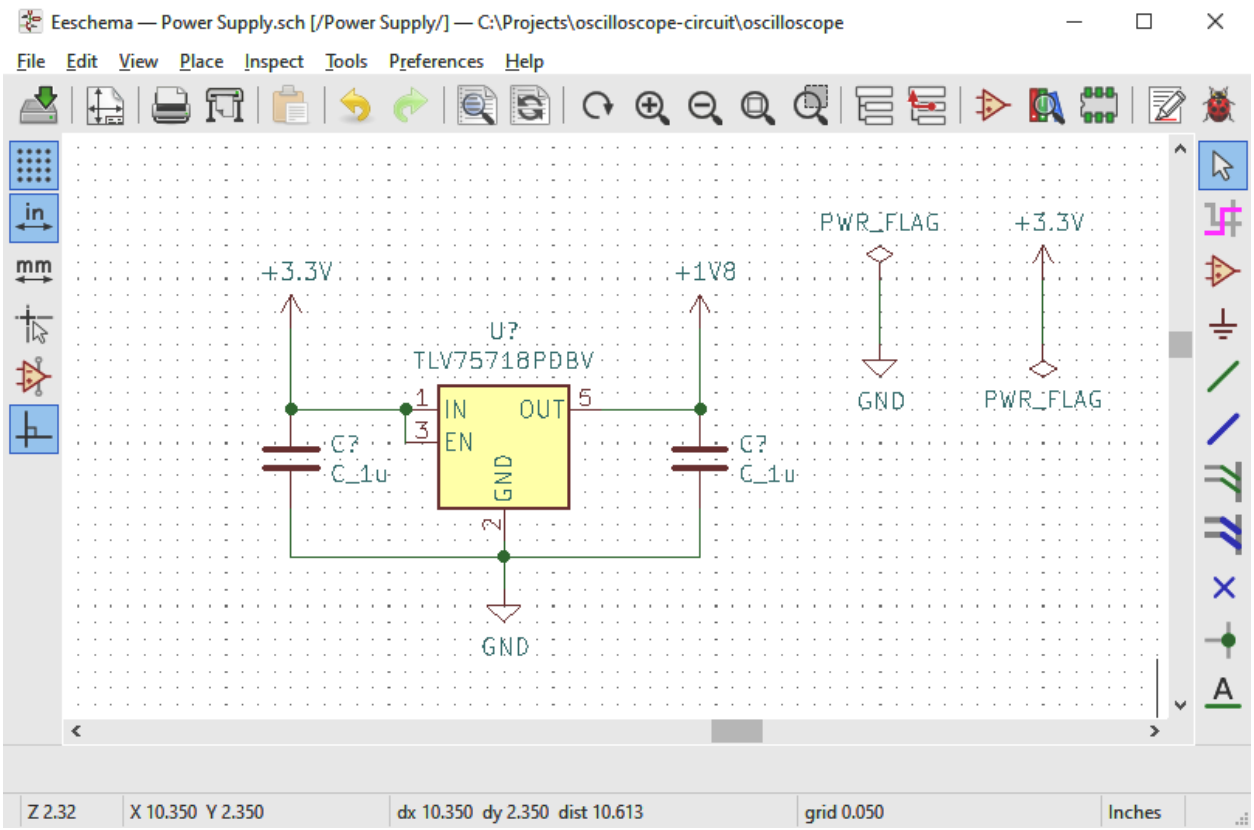

Eeschema — Power Supply.sch [/Power Supply/] — C:\Projects\oscilloscope-circuit\oscilloscope [no file]
File Edit View Place Inspect Tools Preferences Help
Z 1.07
X 5.050 Y 1.900
dx 5.050 dy 1.900 dist 5.396
grid 0.050
Inches

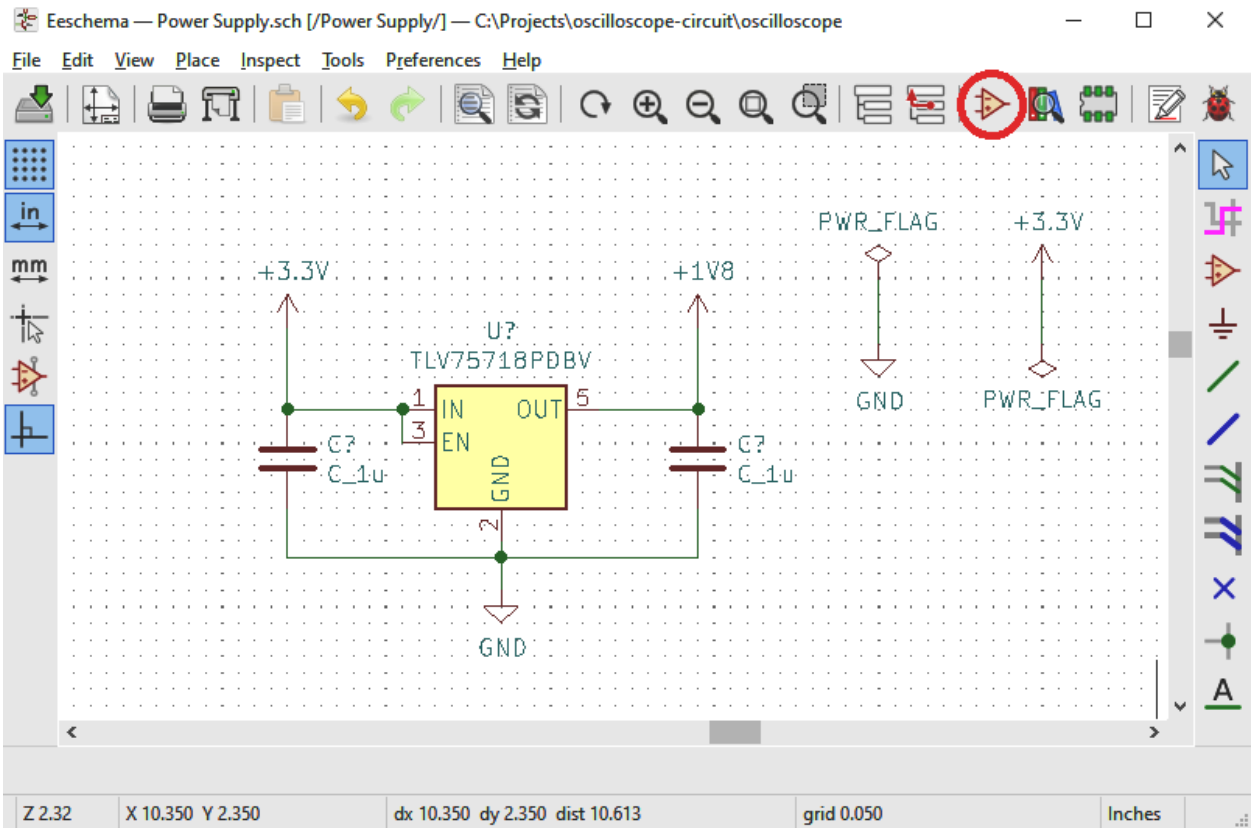

Eeschema — Power Supply.sch [/Power Supply/] — C:\Projects\oscilloscope-circuit\oscilloscope [no file]
File Edit View Place Inspect Tools Preferences Help
4
5
+3.3V
GND
Reference #PWR?
Power symbol +3.3V
Name +3.3V
Alias of +3V3
Library power
Footprint <Unknown>
Description Power symbol creates a global label with name "+3.3V"
Key words power-flag
File C:\Proj...
Z 2.23
X 8.350 Y 0.850
dx 8.350 dy 0.850 dist 8.393
grid 0.050
Inches
Add component

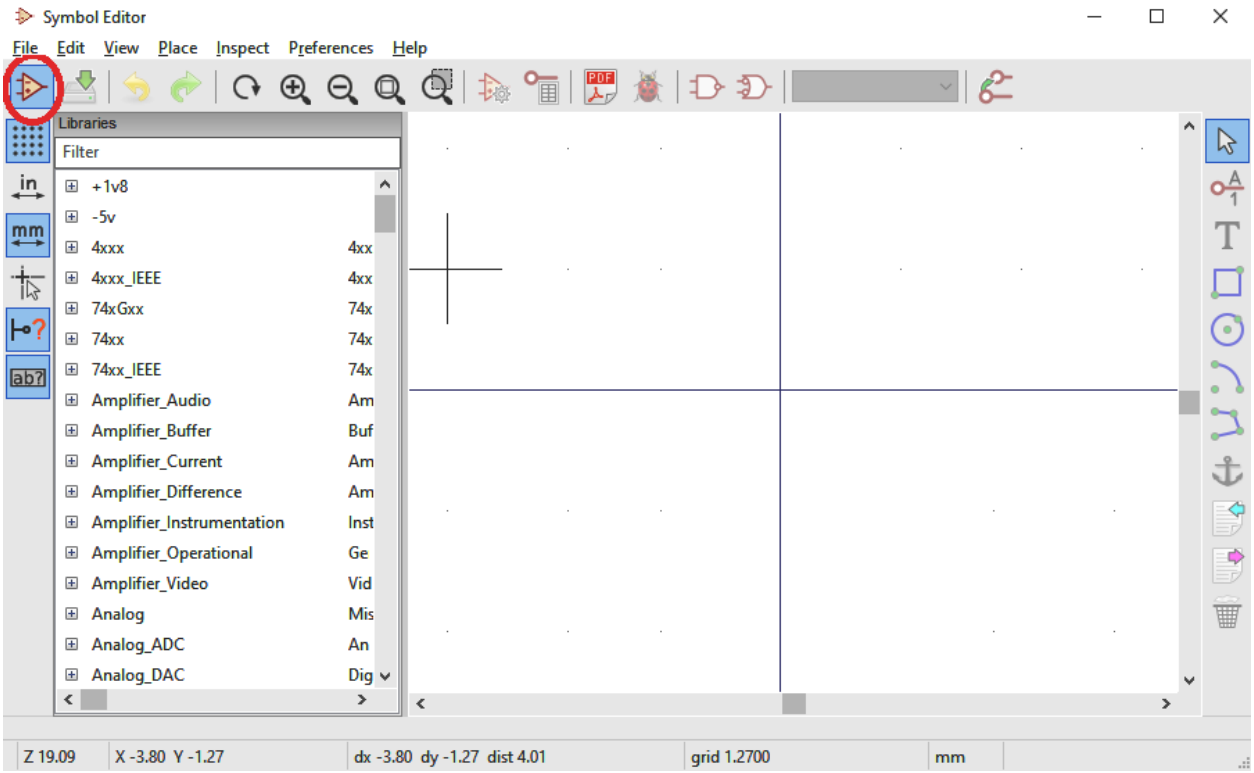

Eeschema — Power Supply.sch [/Power Supply/] — C:\Projects\oscilloscope-circuit\oscilloscope [no file]
File Edit View Place Inspect Tools Preferences Help
PWR_FLAG
+3.3V
PWR_FLAG
GND
Reference #FLG?
Power symbol PWR_FLAG
Name PWR_FLAG
Library power
Footprint <Unknown>
Description Special symbol for telling ERC where power comes from
Key words power-flag
File C:\Proj...
Z 2.23
X 10.650 Y 1.900
dx 10.650 dy 1.900 dist 10.818
grid 0.050
Inches

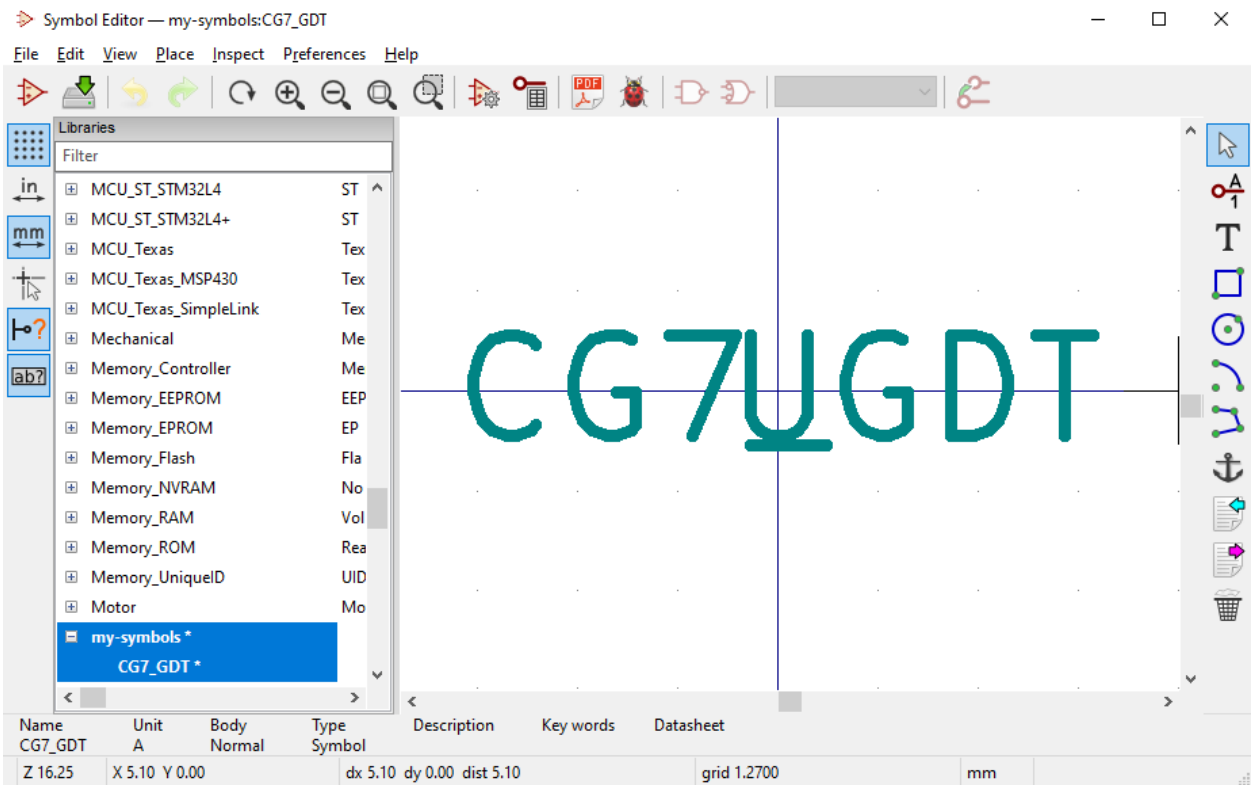

Eeschema — Power Supply.sch [/Power Supply/] — C:\Projects\oscilloscope-circuit\oscilloscope [no file]
File Edit View Place Inspect Tools Preferences Help
PWR_FLAG
+3.3V
GND
PWR_FLAG
File C:\Proj...
Z 2.23
X 7.450 Y 0.300
dx 7.450 dy 0.300 dist 7.456
grid 0.050
Inches

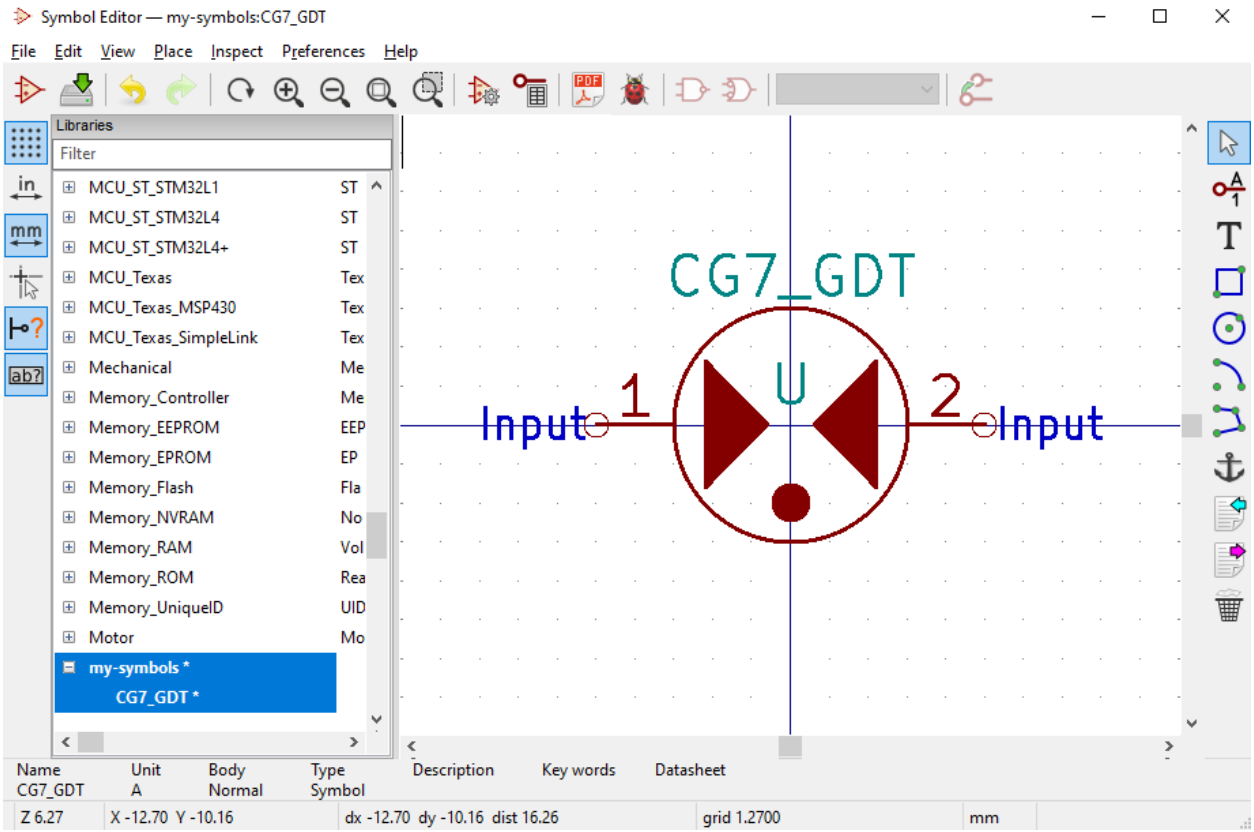

Eeschema — Power Supply.sch [/Power Supply/] — C:\Projects\oscilloscope-circuit\oscilloscope [no file]
File Edit View Place Inspect Tools Preferences Help
PWR_FLAG
+3.3V
GND
PWR_FLAG
File C:\Proj... Z 2.23 X 10.550 Y 1.200 dx 10.550 dy 1.200 dist 10.618 grid 0.050 Inches Add wire

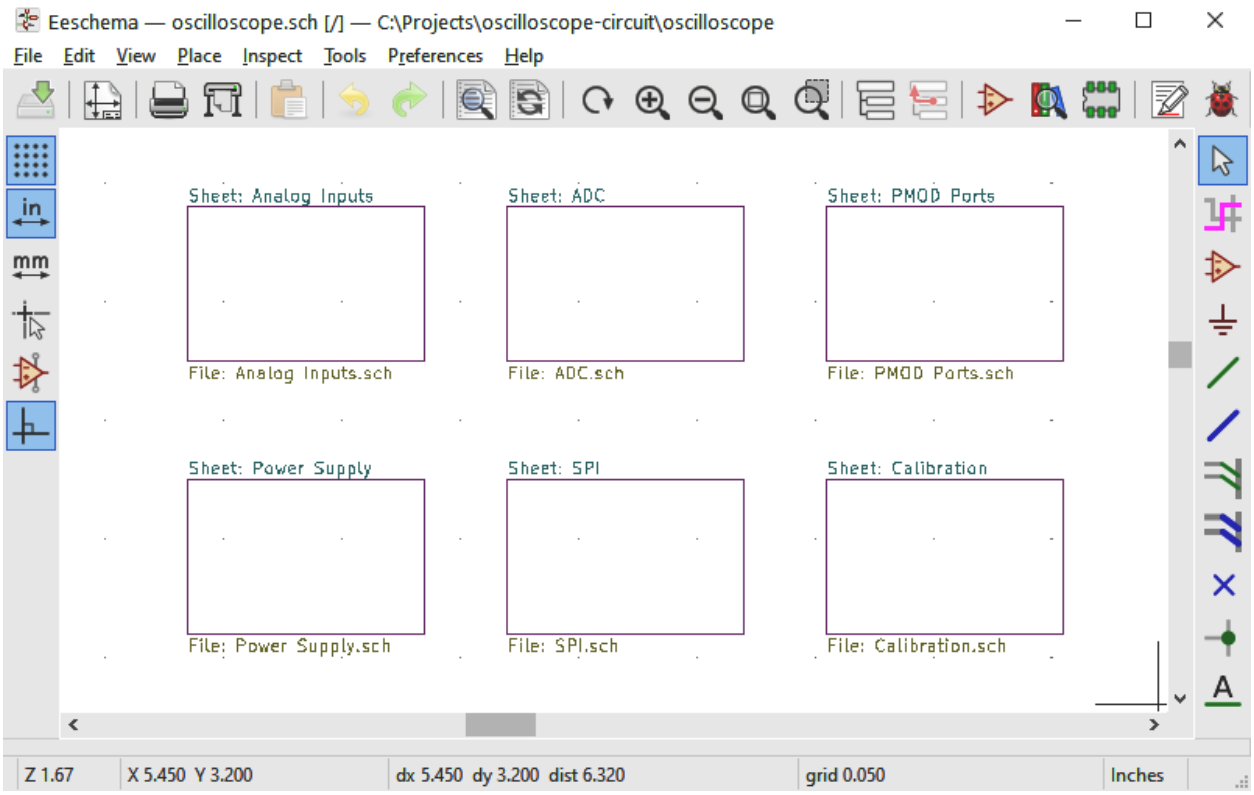

Eeschema — Power Supply.sch [/Power Supply/] — C:\Projects\oscilloscope-circuit\oscilloscope
File Edit View Place Inspect Tools Preferences Help
+3.3V
+1V8
U?
TLV75718PDBV
IN
OUT
EN
GND
C?
C_1u
C?
C_1u
GND
PWR_FLAG
+3.3V
GND
PWR_FLAG
Z 2.32 X 10.350 Y 2.350 dx 10.350 dy 2.350 dist 10.613 grid 0.050 Inches

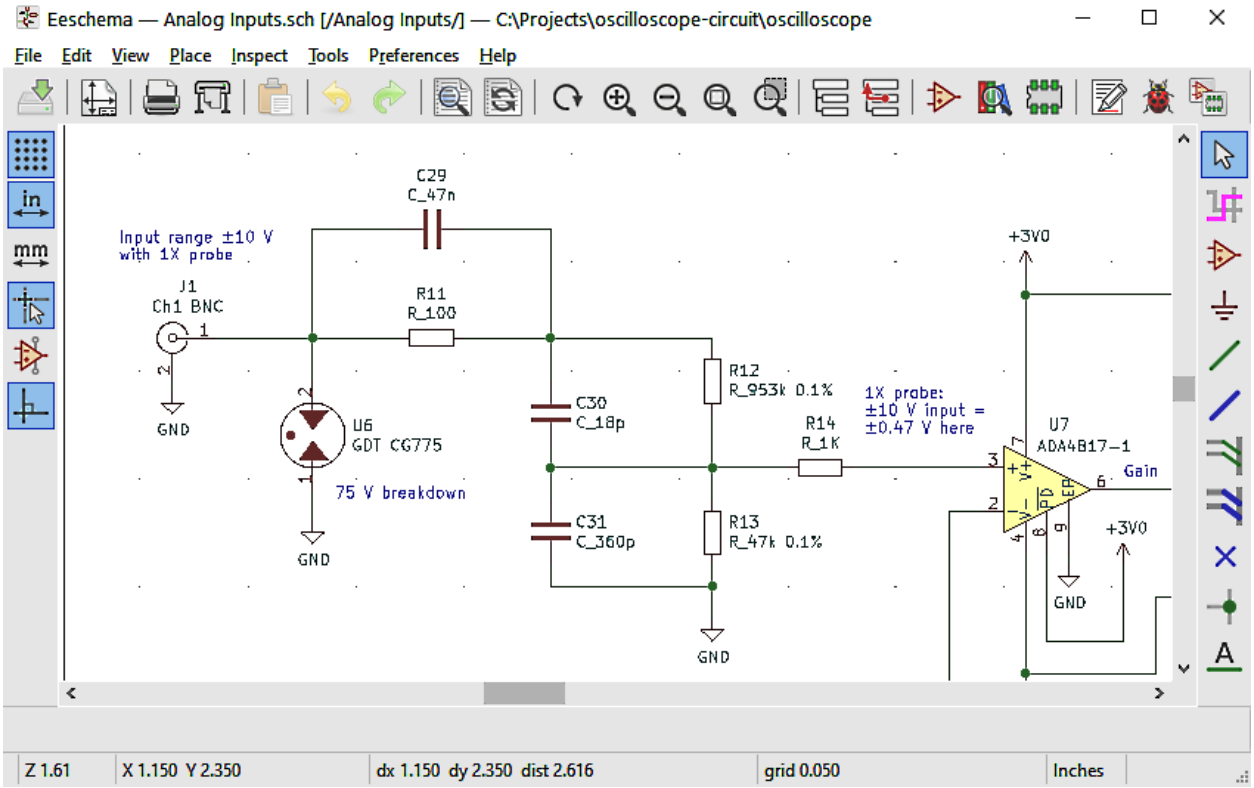

Eeschema — Power Supply.sch [/Power Supply/] — C:\Projects\oscilloscope-circuit\oscilloscope
File Edit View Place Inspect Tools Preferences Help
+3.3V
+1V8
U?
TLV75718PDBV
IN
OUT
EN
GND
C?
C_1u
C?
C_1u
PWR_FLAG
+3.3V
GND
PWR_FLAG
GND
Z 2.32
X 10.350 Y 2.350
dx 10.350 dy 2.350 dist 10.613
grid 0.050
Inches

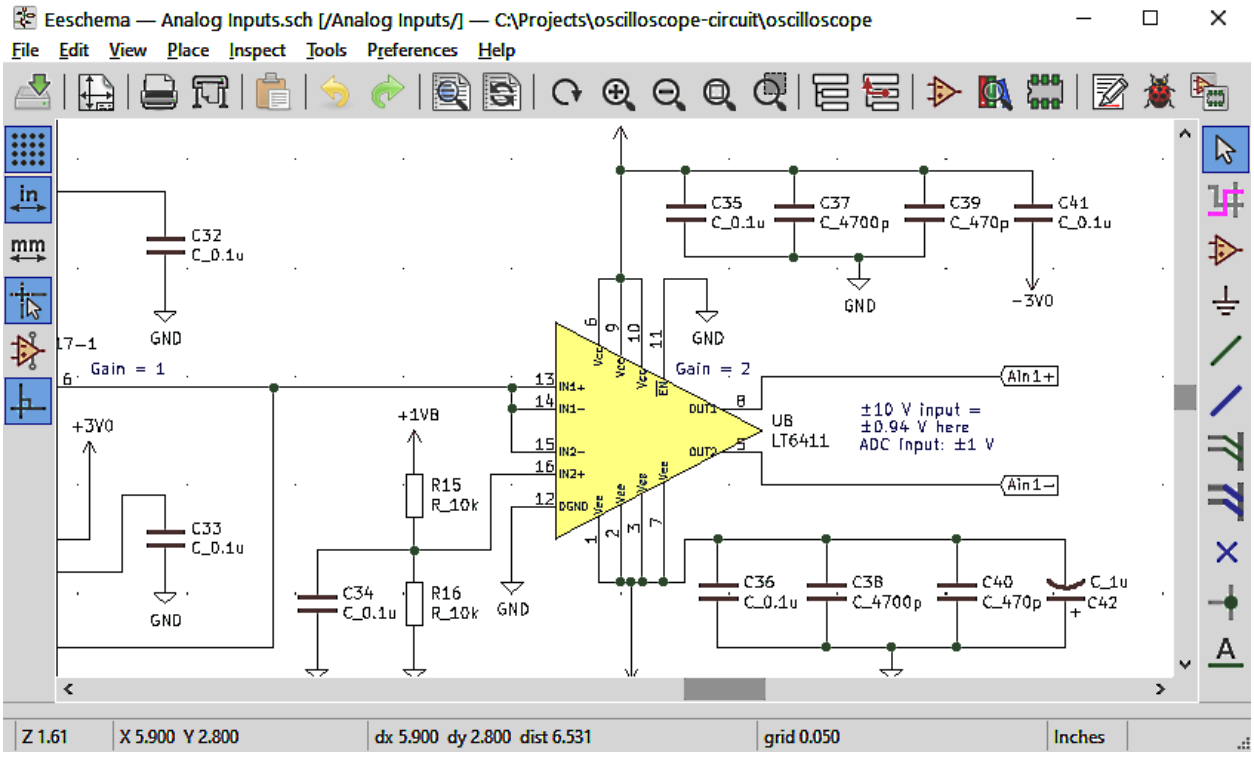

Symbol Editor
File Edit View Place Inspect Preferences Help
Libraries
Filter
+1v8
-5v
4xxx
4xxx_IEEE
74xGxx
74xx
74xx_IEEE
Amplifier_Audio
Amplifier_Buffer
Amplifier_Current
Amplifier_Difference
Amplifier_Instrumentation
Amplifier_Operational
Amplifier_Video
Analog
Analog_ADC
Analog_DAC
Z 19.09
X -3.80 Y -1.27
dx -3.80 dy -1.27 dist 4.01
grid 1.2700
mm

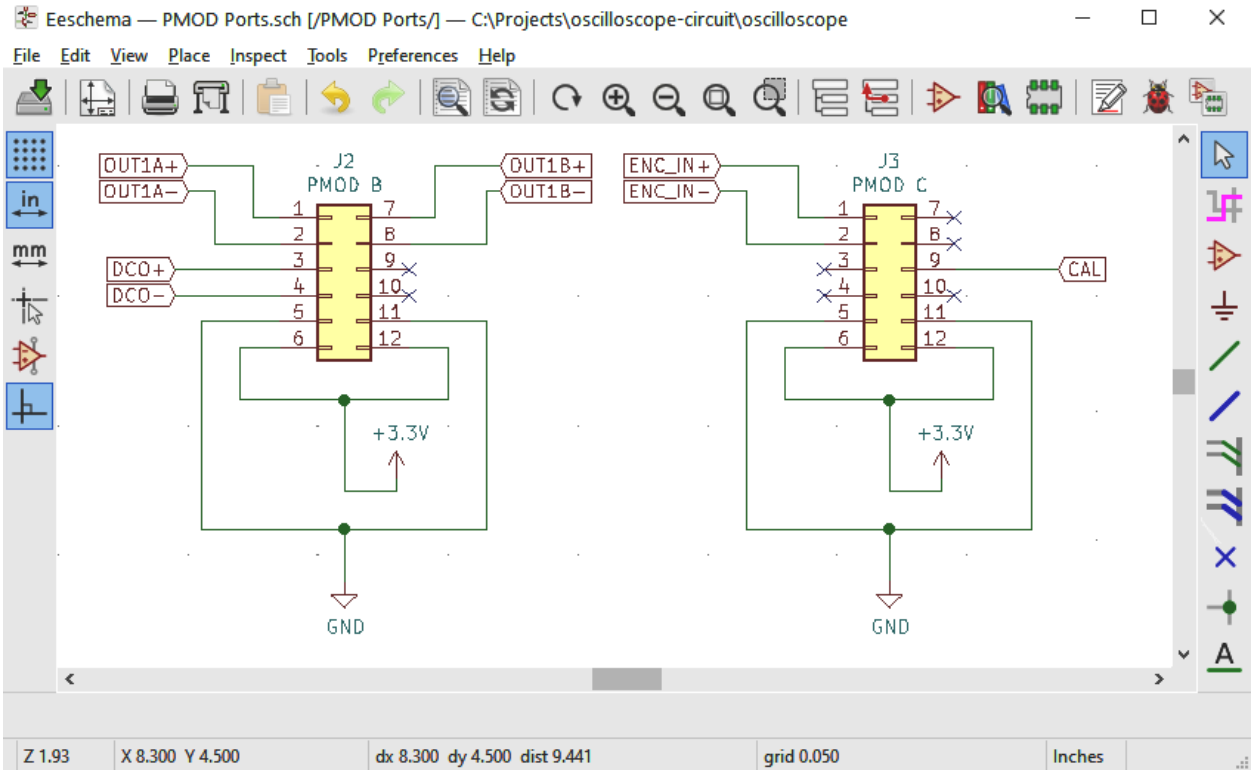

Symbol Editor — my-symbols:CG7_GDT
File Edit View Place Inspect Preferences Help
Libraries
Filter
MCU_ST_STM32L4
MCU_ST_STM32L4+
MCU_Texas
MCU_Texas_MSP430
MCU_Texas_SimpleLink
Mechanical
Memory_Controller
Memory_EEPROM
Memory_EPROM
Memory_Flash
Memory_NVRAM
Memory_RAM
Memory_ROM
Memory_UniqueID
Motor
my-symbols *
CG7_GDT *
CG7_GDT
Name CG7_GDT
Unit A
Body Normal
Type Symbol
Description
Key words
Datasheet
Z 16.25
X 5.10 Y 0.00
dx 5.10 dy 0.00 dist 5.10
grid 1.2700
mm

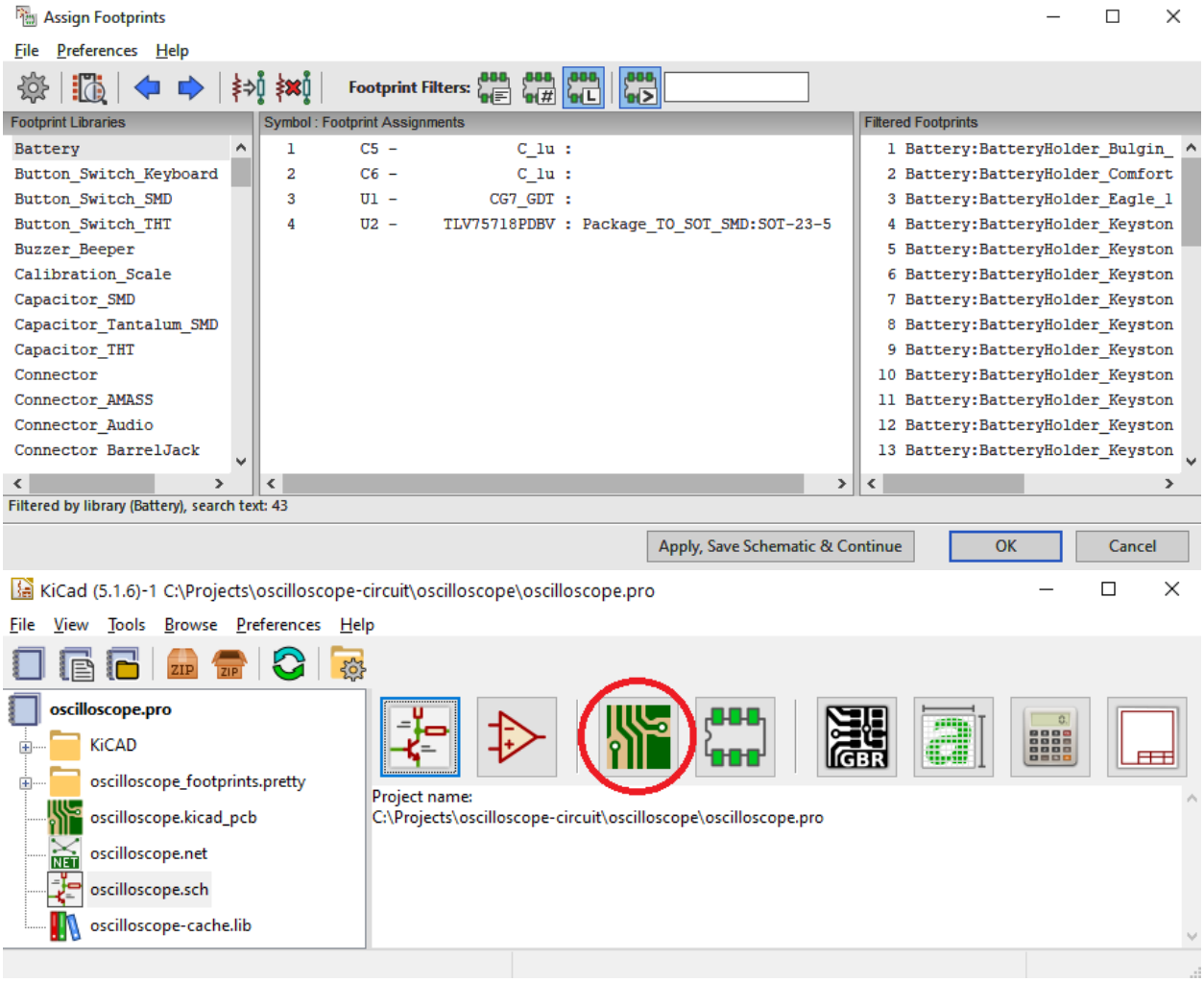

Symbol Editor — my-symbols:CG7_GDT
File Edit View Place Inspect Preferences Help
Libraries
Filter
MCU_ST_STM32L1
MCU_ST_STM32L4
MCU_ST_STM32L4+
MCU_Texas
MCU_Texas_MSP430
MCU_Texas_SimpleLink
Mechanical
Memory_Controller
Memory_EEPROM
Memory_EPROM
Memory_Flash
Memory_NVRAM
Memory_RAM
Memory_ROM
Memory_UniqueID
Motor
my-symbols *
CG7_GDT *
CG7_GDT
Input
1
U
2
Input
Name CG7_GDT
Unit A
Body Normal
Type Symbol
Description
Key words
Datasheet
Z 6.27
X -12.70 Y -10.16
dx -12.70 dy -10.16 dist 16.26
grid 1.2700
mm


Eeschema — oscilloscope.sch [/] — C:\Projects\oscilloscope-circuit\oscilloscope
File Edit View Place Inspect Tools Preferences Help
Sheet: Analog Inputs
File: Analog Inputs.sch
Sheet: ADC
File: ADC.sch
Sheet: PMOD Ports
File: PMOD Ports.sch
Sheet: Power Supply
File: Power Supply.sch
Sheet: SPI
File: SPI.sch
Sheet: Calibration
File: Calibration.sch
Z 1.67
X 5.450 Y 3.200
dx 5.450 dy 3.200 dist 6.320
grid 0.050
Inches

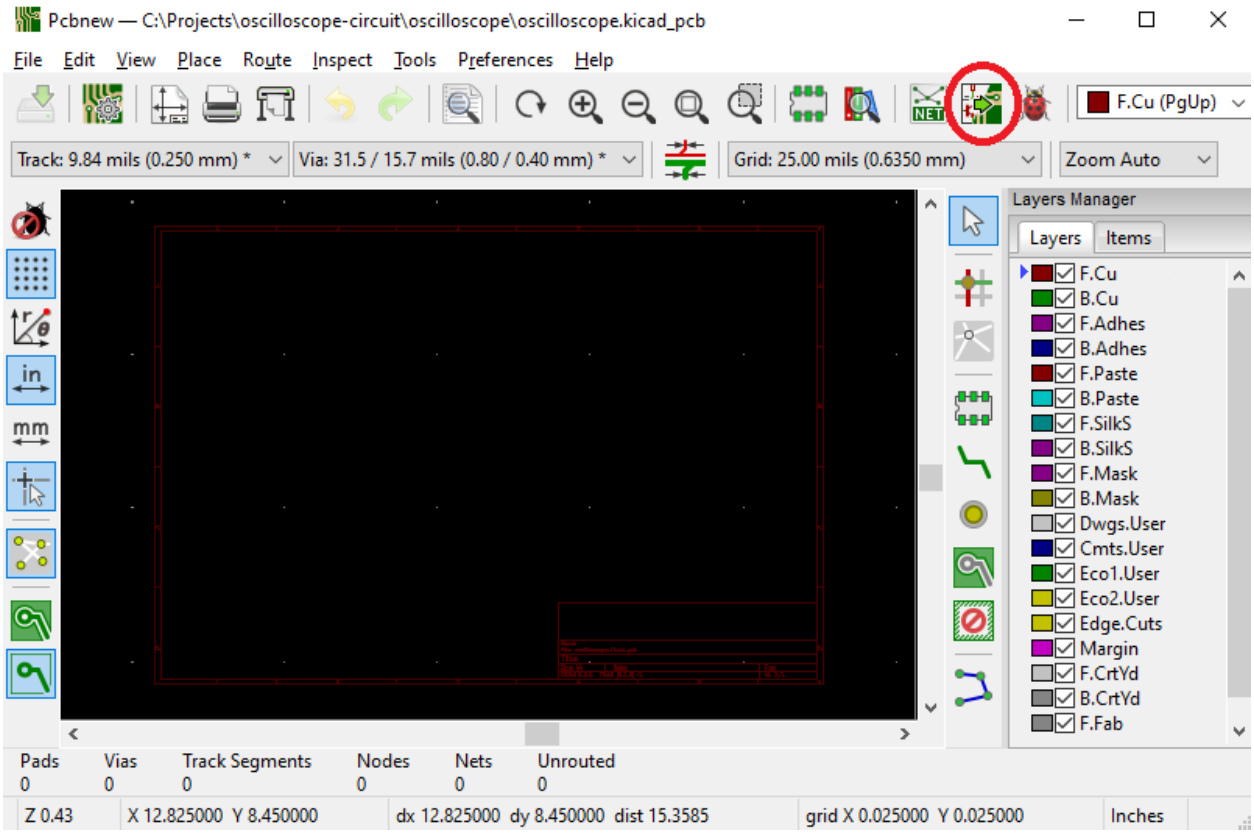

Eeschema — Analog Inputs.sch [/Analog Inputs/] — C:\Projects\oscilloscope-circuit\oscilloscope
File Edit View Place Inspect Tools Preferences Help
C29
C_47n
Input range ±10 V
with 1X probe
J1
Ch1 BNC
R11
R_100
GND
U6
GDT CG775
75 V breakdown
C30
C_18p
C31
C_360p
R12
R_953k 0.1%
R14
R_1K
R13
R_47k 0.1%
1X probe:
±10 V input =
±0.47 V here
+3V0
U7
ADA4817-1
Gain
Z 1.61
X 1.150 Y 2.350
dx 1.150 dy 2.350 dist 2.616
grid 0.050
Inches

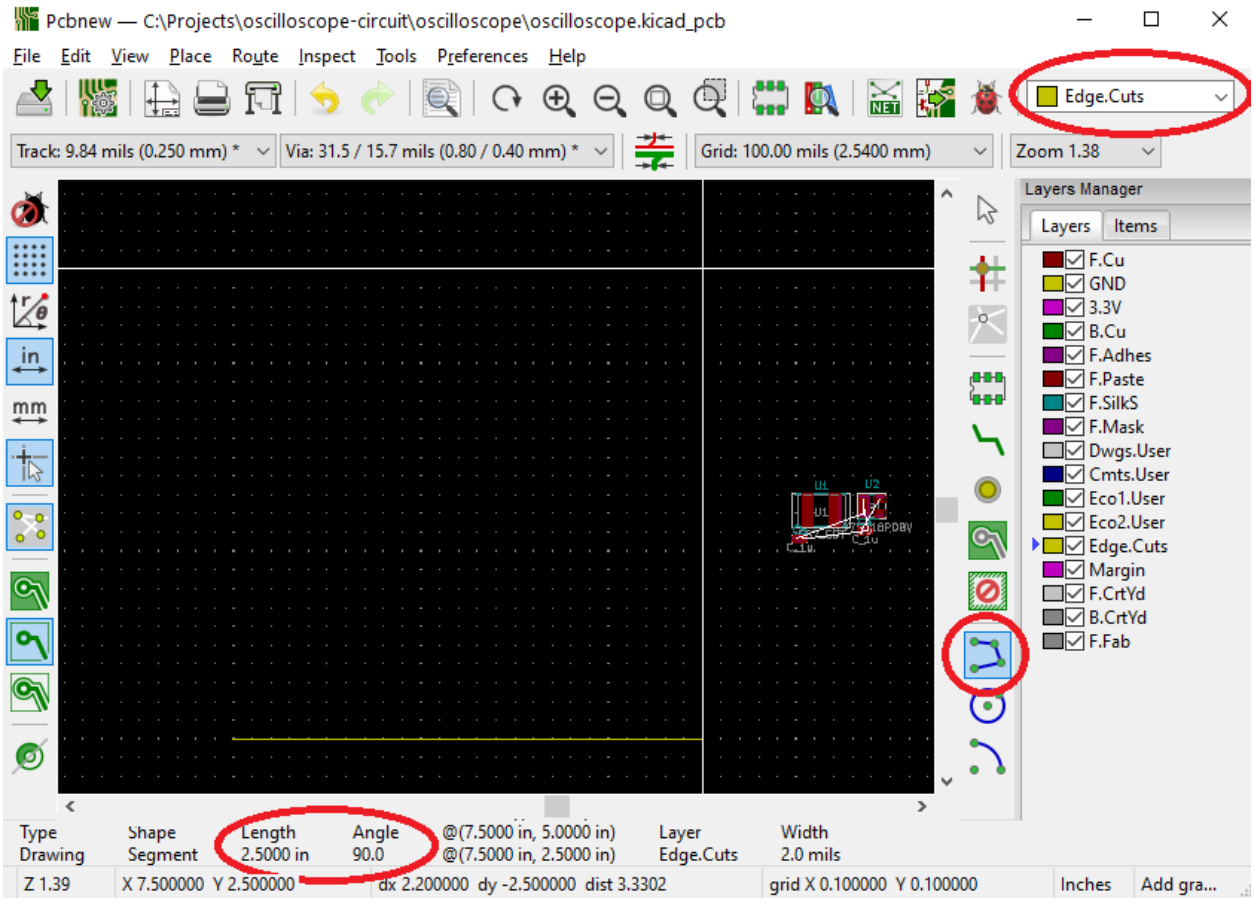

Eeschema — Analog Inputs.sch [/Analog Inputs/] — C:\Projects\oscilloscope-circuit\oscilloscope
File Edit View Place Inspect Tools Preferences Help
C32 C_0.1u
GND
L7-1
Gain = 1
+3V0
C33 C_0.1u
GND
+1VB
R15 R_10k
R16 R_10k
C34 C_0.1u
GND
C35 C_0.1u
C37 C_4700p
C39 C_470p
C41 C_0.1u
GND
-3V0
GND
Gain = 2
IN1+
IN1-
IN2-
IN2+
DGND
Vcc
Vee
EN
OUT1
OUT2
UB
LT6411
±10 V input =
±0.94 V here
ADC Input: ±1 V
Ain1+
Ain1-
C36 C_0.1u
C38 C_4700p
C40 C_470p
C_1u C42
Z 1.61
X 5.900 Y 2.800
dx 5.900 dy 2.800 dist 6.531
grid 0.050
Inches

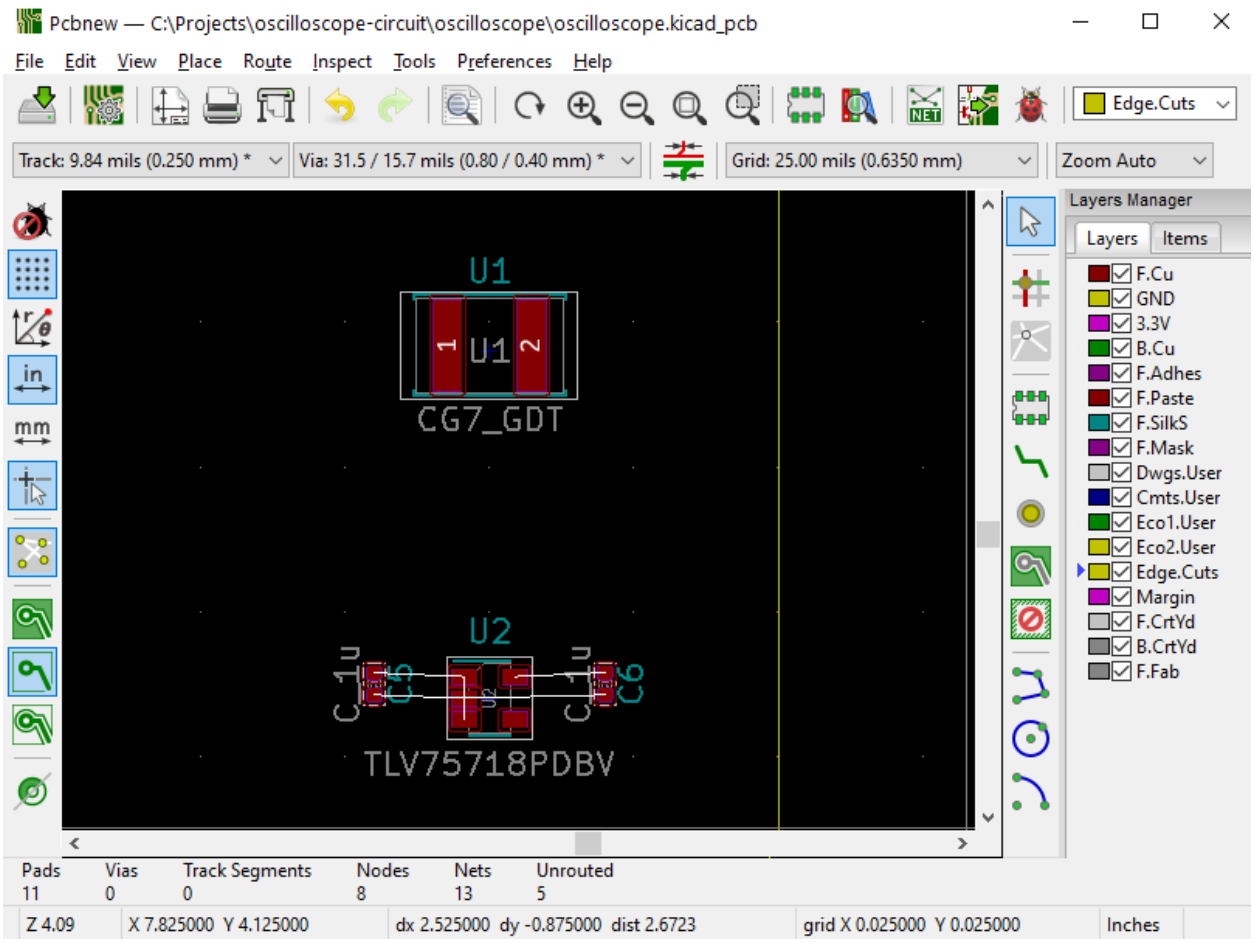

Eeschema — PMOD Ports.sch [/PMOD Ports/] — C:\Projects\oscilloscope-circuit\oscilloscope
File Edit View Place Inspect Tools Preferences Help
OUT1A+
OUT1A-
J2
PMOD B
OUT1B+
OUT1B-
DCO+
DCO-
+3.3V
GND
ENC_IN+
ENC_IN-
J3
PMOD C
CAL
+3.3V
GND
Z 1.93
X 8.300 Y 4.500
dx 8.300 dy 4.500 dist 9.441
grid 0.050
Inches

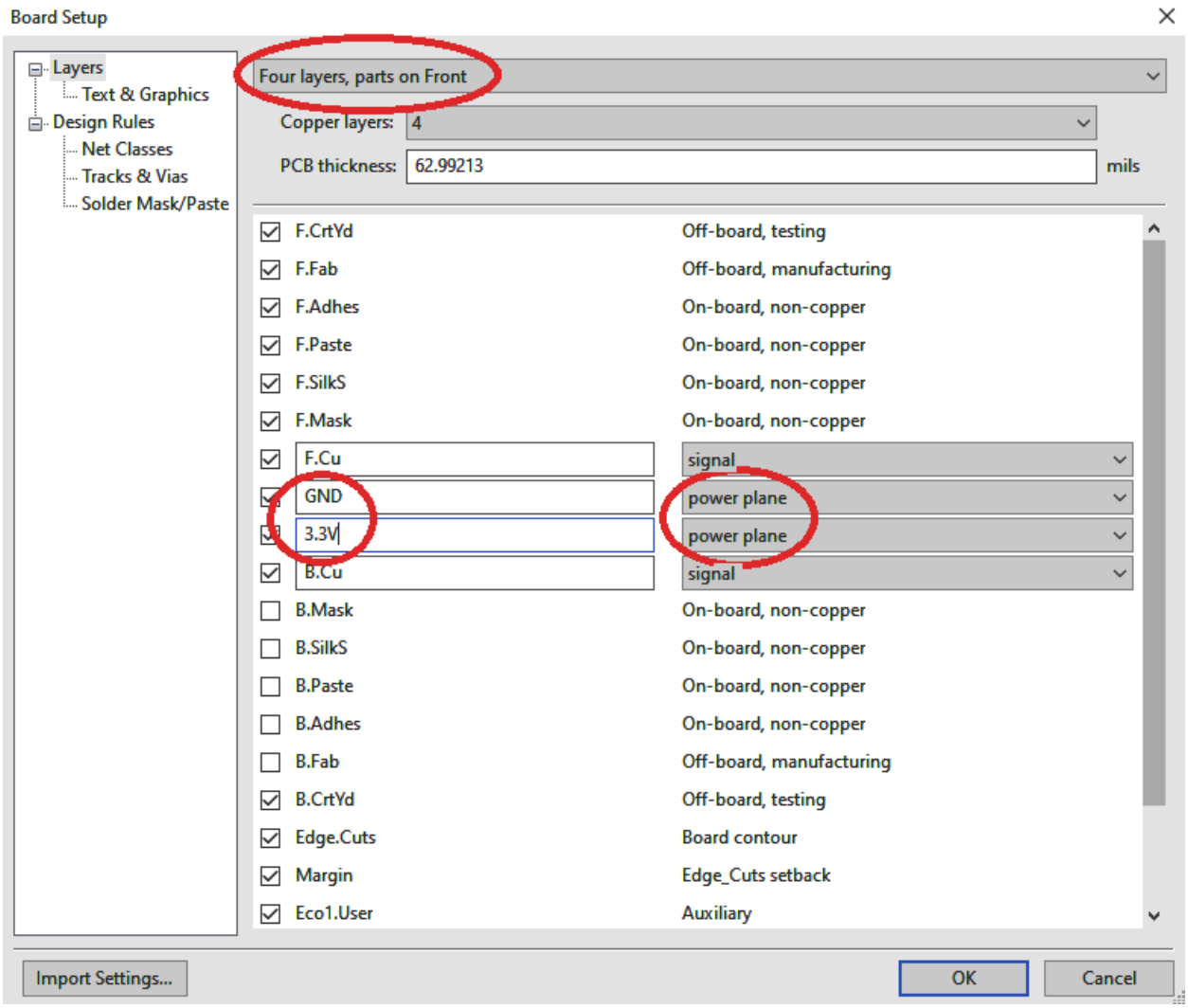

Assign Footprints
File Preferences Help
Footprint Filters:
Footprint Libraries
Battery
Button_Switch_Keyboard
Button_Switch_SMD
Button_Switch_THT
Buzzer_Beeper
Calibration_Scale
Capacitor_SMD
Capacitor_Tantalum_SMD
Capacitor_THT
Connector
Connector_AMASS
Connector_Audio
Connector_BarrelJack
Symbol : Footprint Assignments
1 C5 - C_1u :
2 C6 - C_1u :
3 U1 - CG7_GDT :
4 U2 - TLV75718PDBV : Package_TO_SOT_SMD:SOT-23-5
Filtered Footprints
1 Battery:BatteryHolder_Bulgin_
2 Battery:BatteryHolder_Comfort
3 Battery:BatteryHolder_Eagle_1
4 Battery:BatteryHolder_Keyston
5 Battery:BatteryHolder_Keyston
6 Battery:BatteryHolder_Keyston
7 Battery:BatteryHolder_Keyston
8 Battery:BatteryHolder_Keyston
9 Battery:BatteryHolder_Keyston
10 Battery:BatteryHolder_Keyston
11 Battery:BatteryHolder_Keyston
12 Battery:BatteryHolder_Keyston
13 Battery:BatteryHolder_Keyston
Filtered by library (Battery), search text: 43
Apply, Save Schematic & Continue
OK
Cancel

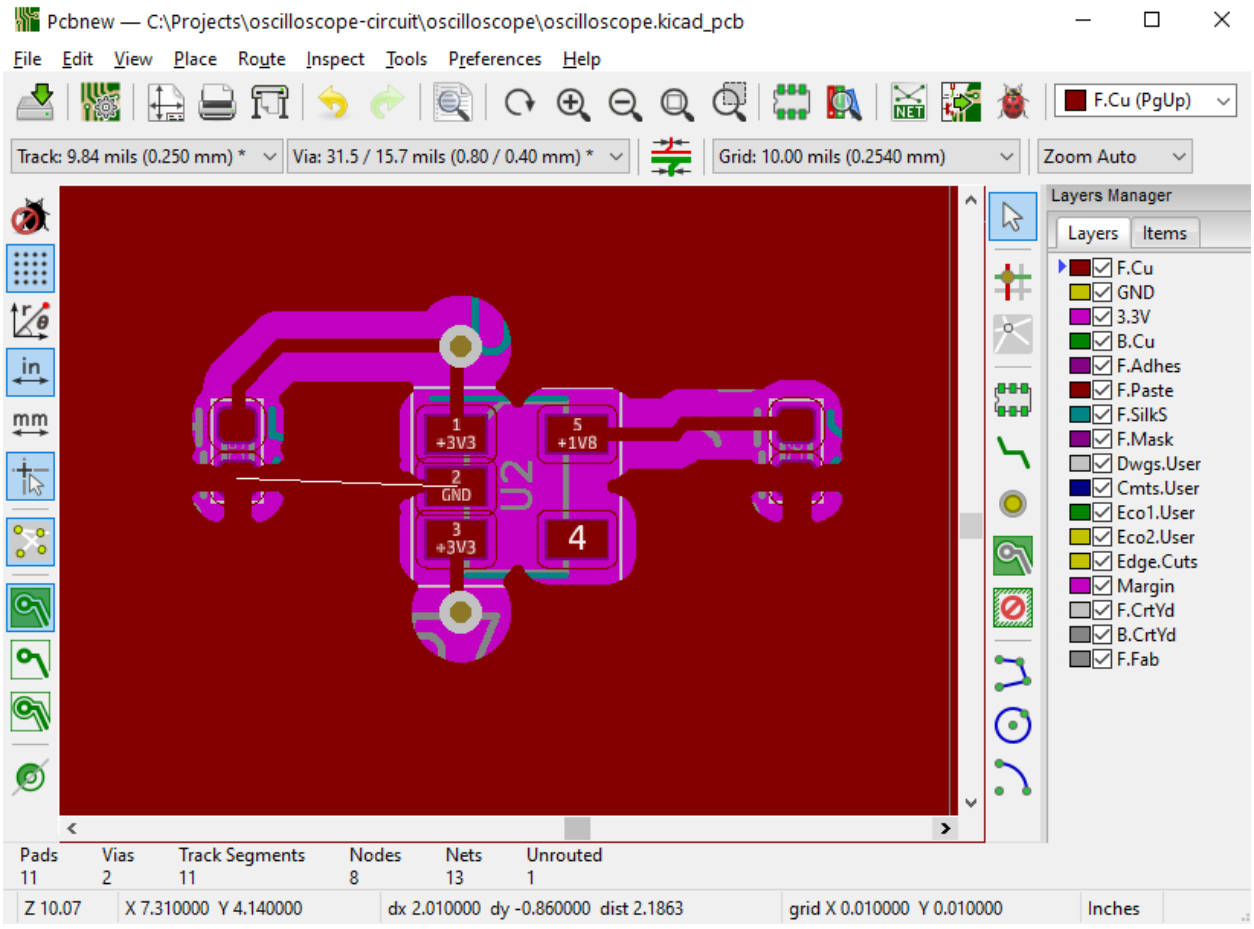
KiCad (5.1.6)-1 C:\Projects\oscilloscope-circuit\oscilloscope\oscilloscope.pro
File View Tools Browse Preferences Help
oscilloscope.pro
KiCAD
oscilloscope_footprints.pretty
oscilloscope.kicad_pcb
oscilloscope.net
oscilloscope.sch
oscilloscope-cache.lib
Project name:
C:\Projects\oscilloscope-circuit\oscilloscope\oscilloscope.pro

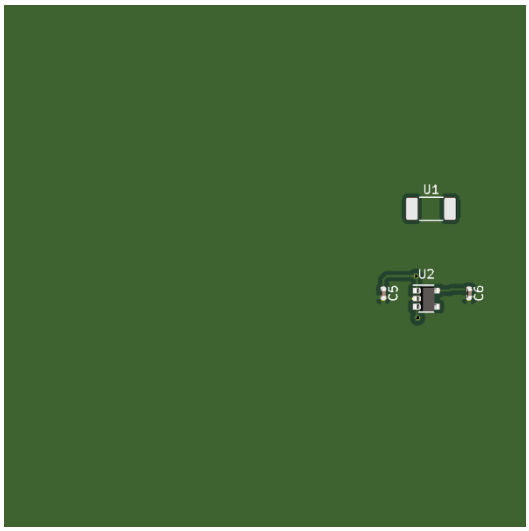

Pcbnew — C:\Projects\oscilloscope-circuit\oscilloscope\oscilloscope.kicad_pcb
File Edit View Place Route Inspect Tools Preferences Help
F.Cu (PgUp)
Track: 9.84 mils (0.250 mm) *
Via: 31.5 / 15.7 mils (0.80 / 0.40 mm) *
Grid: 25.00 mils (0.6350 mm)
Zoom Auto
Layers Manager
Layers
Items
F.Cu
B.Cu
F.Adhes
B.Adhes
F.Paste
B.Paste
F.SilkS
B.SilkS
F.Mask
B.Mask
Dwgs.User
Cmts.User
Eco1.User
Eco2.User
Edge.Cuts
Margin
F.CrtYd
B.CrtYd
F.Fab
Pads
0
Vias
0
Track Segments
0
Nodes
0
Nets
0
Unrouted
0
Z 0.43
X 12.825000 Y 8.450000
dx 12.825000 dy 8.450000 dist 15.3585
grid X 0.025000 Y 0.025000
Inches

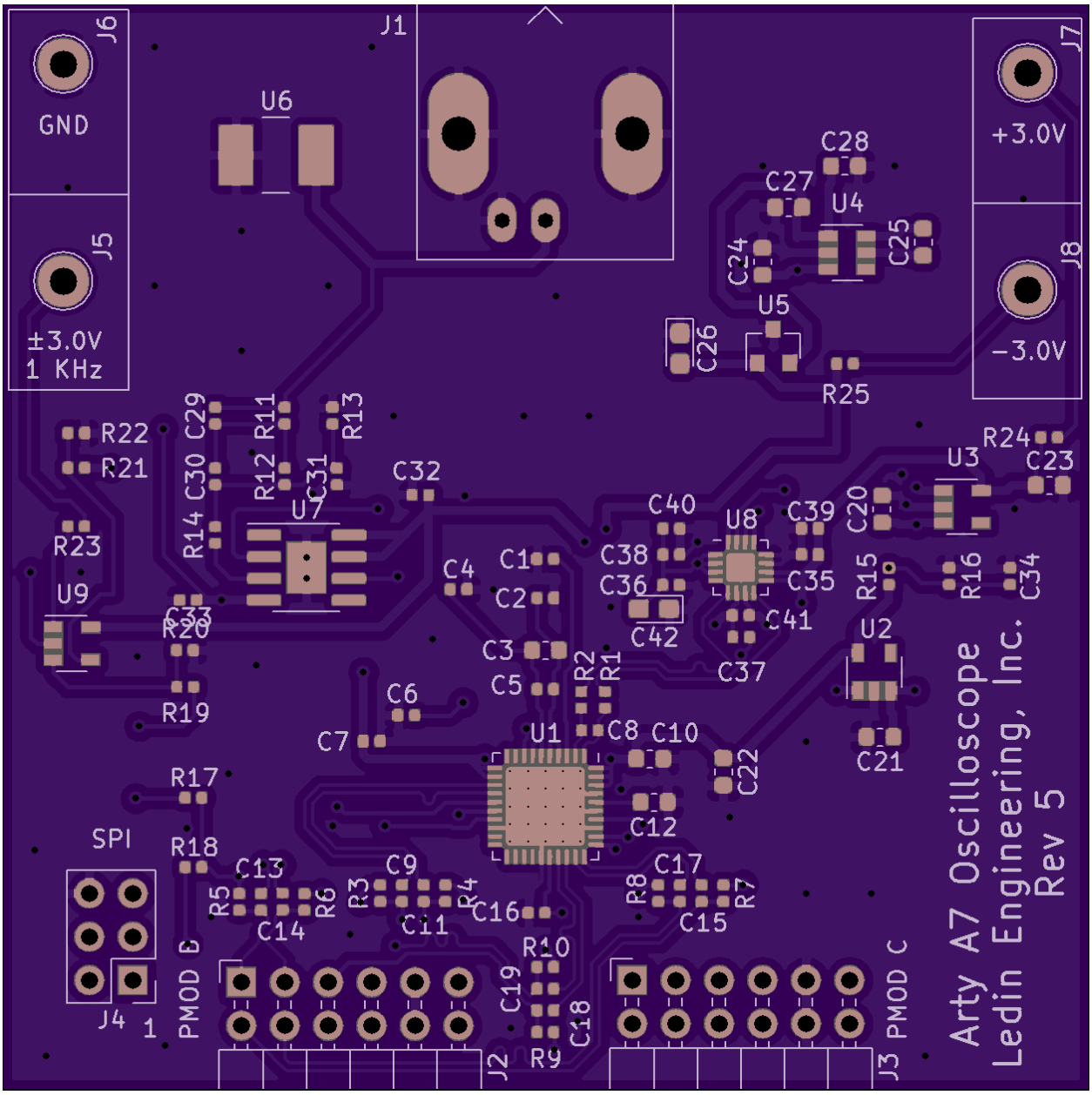

Pcbnew — C:\Projects\oscilloscope-circuit\oscilloscope\oscilloscope.kicad_pcb
File Edit View Place Route Inspect Tools Preferences Help
Edge.Cuts
Track: 9.84 mils (0.250 mm) *
Via: 31.5 / 15.7 mils (0.80 / 0.40 mm) *
Grid: 100.00 mils (2.5400 mm)
Zoom 1.38
Layers Manager
Layers Items
F.Cu
GND
3.3V
B.Cu
F.Adhes
F.Paste
F.SilkS
F.Mask
Dwgs.User
Cmts.User
Eco1.User
Eco2.User
Edge.Cuts
Margin
F.CrtYd
B.CrtYd
F.Fab
Type Shape Length Angle @(7.5000 in, 5.0000 in) Layer Width
Drawing Segment 2.5000 in 90.0 @(7.5000 in, 2.5000 in) Edge.Cuts 2.0 mils
Z 1.39 X 7.500000 Y 2.500000 dx 2.200000 dy -2.500000 dist 3.3302 grid X 0.100000 Y 0.100000 Inches Add gra...


Pcbnew — C:\Projects\oscilloscope-circuit\oscilloscope\oscilloscope.kicad_pcb
File Edit View Place Route Inspect Tools Preferences Help
Edge.Cuts
Track: 9.84 mils (0.250 mm) *
Via: 31.5 / 15.7 mils (0.80 / 0.40 mm) *
Grid: 25.00 mils (0.6350 mm)
Zoom Auto
Layers Manager
Layers Items
F.Cu
GND
3.3V
B.Cu
F.Adhes
F.Paste
F.SilkS
F.Mask
Dwgs.User
Cmts.User
Eco1.User
Eco2.User
Edge.Cuts
Margin
F.CrtYd
B.CrtYd
F.Fab
U1
1
U1
2
CG7_GDT
U2
C13
C5
C6
TLV75718PDBV
Pads 11
Vias 0
Track Segments 0
Nodes 8
Nets 13
Unrouted 5
Z 4.09
X 7.825000 Y 4.125000
dx 2.525000 dy -0.875000 dist 2.6723
grid X 0.025000 Y 0.025000
Inches

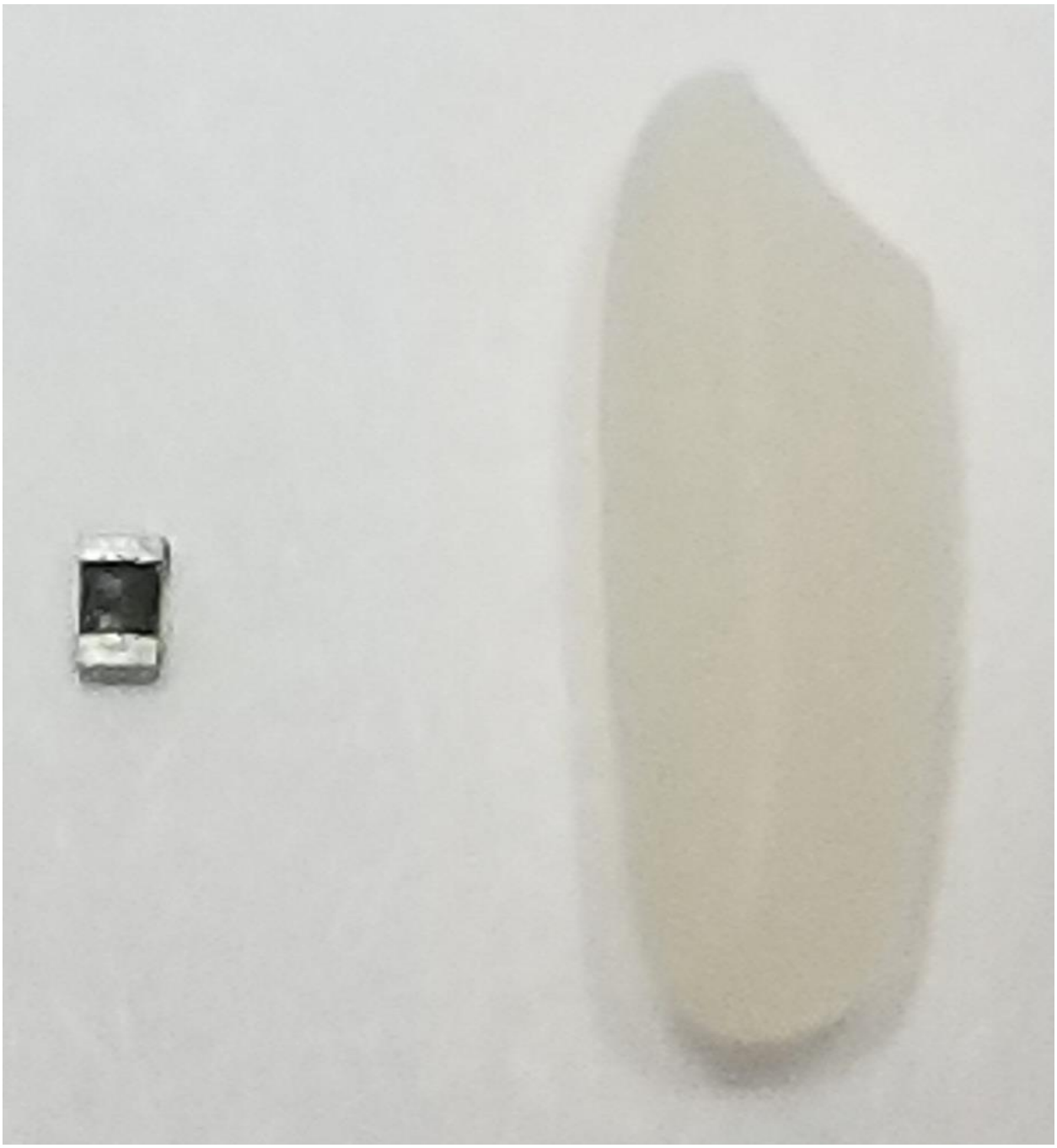

Board Setup
Layers
Text & Graphics
Design Rules
Net Classes
Tracks & Vias
Solder Mask/Paste
Four layers, parts on Front
Copper layers: 4
PCB thickness: 62.99213
mils
F.CrtYd Off-board, testing
F.Fab Off-board, manufacturing
F.Adhes On-board, non-copper
F.Paste On-board, non-copper
F.SilkS On-board, non-copper
F.Mask On-board, non-copper
F.Cu signal
GND power plane
3.3V power plane
B.Cu signal
B.Mask On-board, non-copper
B.SilkS On-board, non-copper
B.Paste On-board, non-copper
B.Adhes On-board, non-copper
B.Fab Off-board, manufacturing
B.CrtYd Off-board, testing
Edge.Cuts Board contour
Margin Edge_Cuts setback
Eco1.User Auxiliary
Import Settings...
OK
Cancel


Pcbnew — C:\Projects\oscilloscope-circuit\oscilloscope\oscilloscope.kicad_pcb
File Edit View Place Route Inspect Tools Preferences Help
F.Cu (PgUp)
Track: 9.84 mils (0.250 mm) *
Via: 31.5 / 15.7 mils (0.80 / 0.40 mm) *
Grid: 10.00 mils (0.2540 mm)
Zoom Auto
Layers Manager
Layers
Items
F.Cu
GND
3.3V
B.Cu
F.Adhes
F.Paste
F.SilkS
F.Mask
Dwgs.User
Cmts.User
Eco1.User
Eco2.User
Edge.Cuts
Margin
F.CrtYd
B.CrtYd
F.Fab
1
+3V3
2
GND
3
+3V3
4
5
+1V8
U2
Pads
11
Vias
2
Track Segments
11
Nodes
8
Nets
13
Unrouted
1
Z 10.07
X 7.310000 Y 4.140000
dx 2.010000 dy -0.860000 dist 2.1863
grid X 0.010000 Y 0.010000
Inches

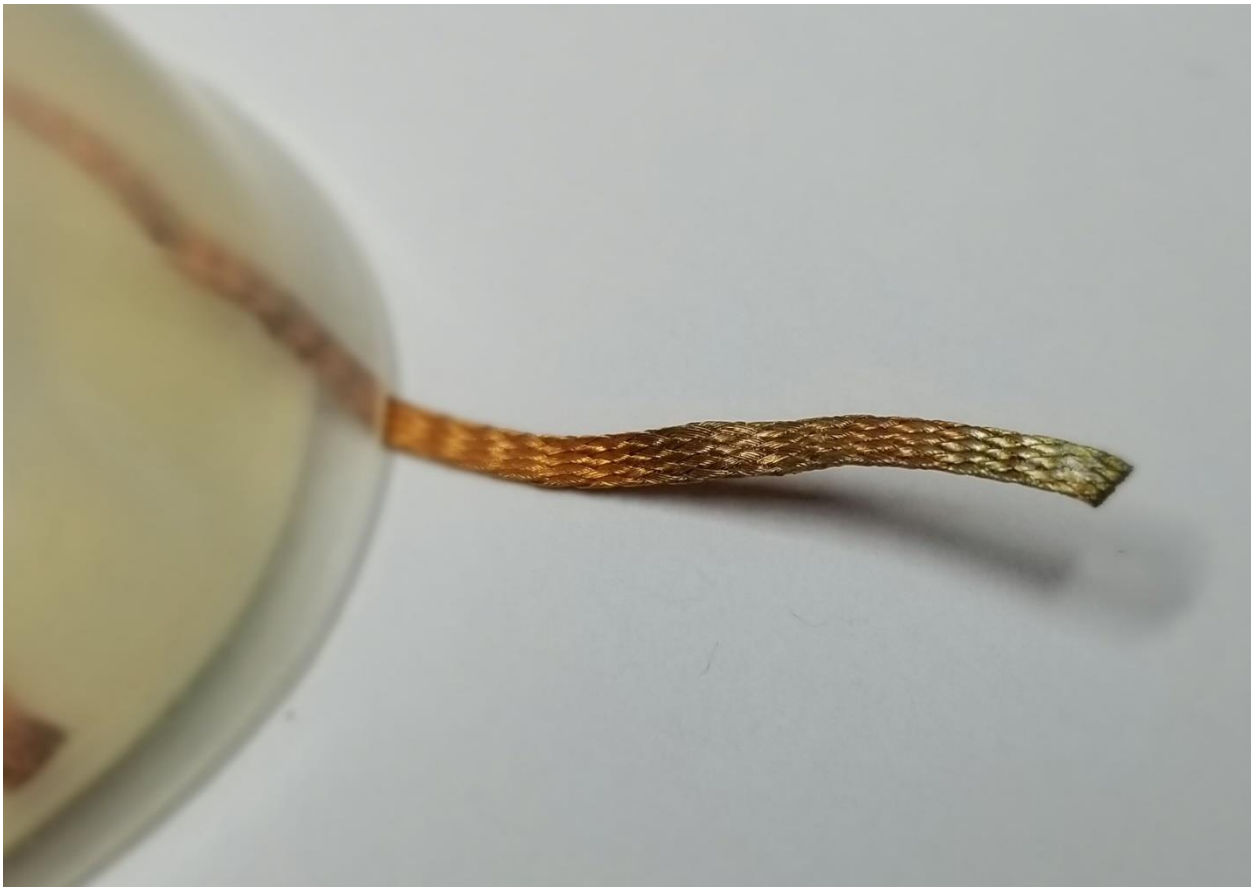

U1
U2
C5
C6

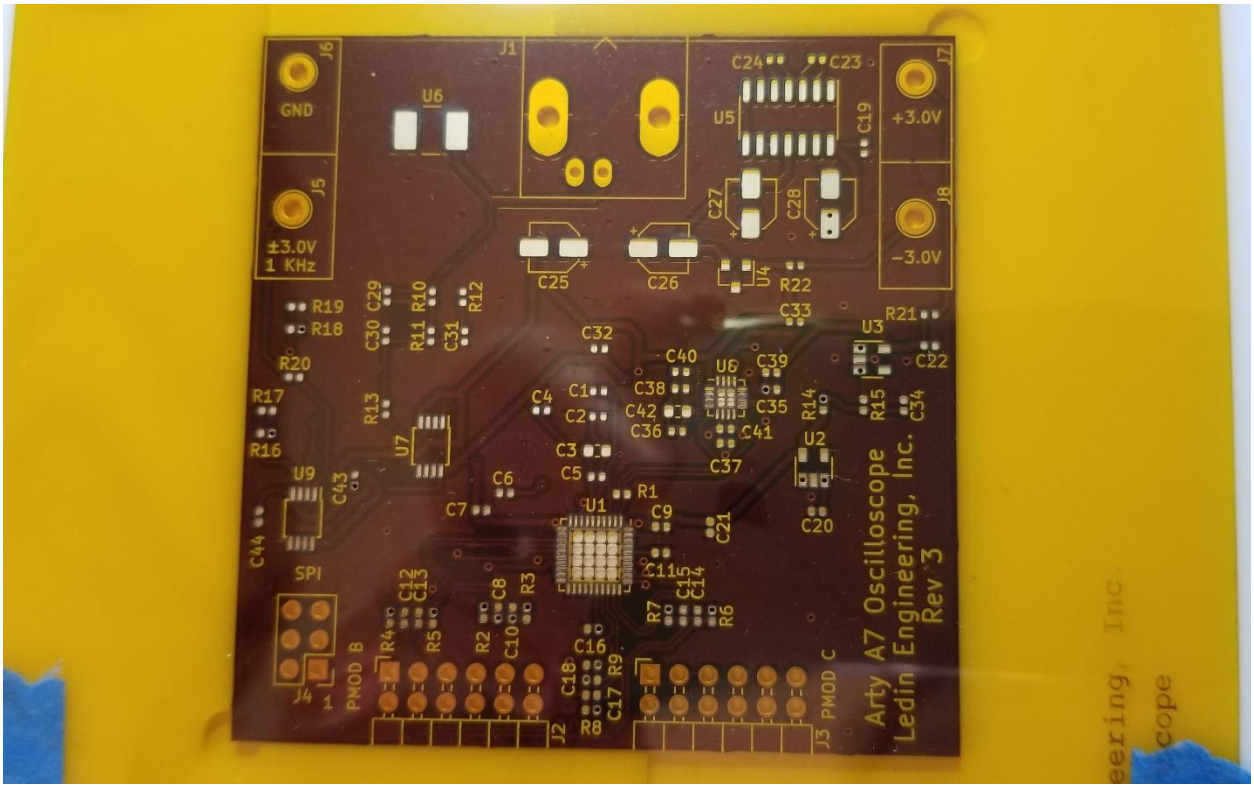

J6
GND
J5
±3.0V
1 KHz
J1
U6
J7
+3.0V
J8
-3.0V
C28
C27
U4
C25
C24
U5
C26
R25
R22
R21
C29
R11
R13
C30
R12
C31
C32
U7
R14
R23
U9
C33
R20
R19
C4
C1
C2
C40
C38
C36
C42
U8
C39
C35
C41
C37
C20
U3
R24
C23
R15
R16
C34
U2
C21
C3
C5
R2
R1
C6
C7
U1
C8
C10
C22
C12
R17
R18
SPI
J4
1
C13
C9
C17
R5
R6
R3
R4
C14
C11
C16
R8
R7
C15
R10
C19
C18
R9
PMOD B
J2
PMOD C
J3
Arty A7 Oscilloscope
Ledin Engineering, Inc.
Rev 5

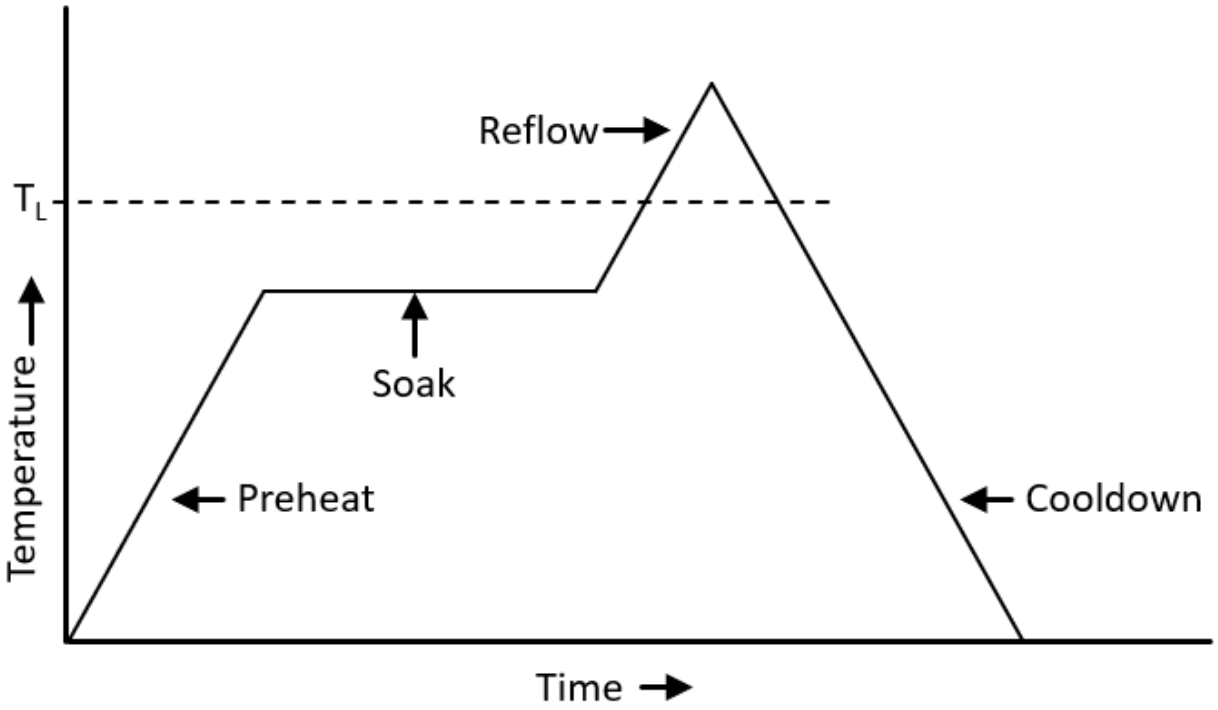
Chapter 7: Building High-Performance Digital Circuits

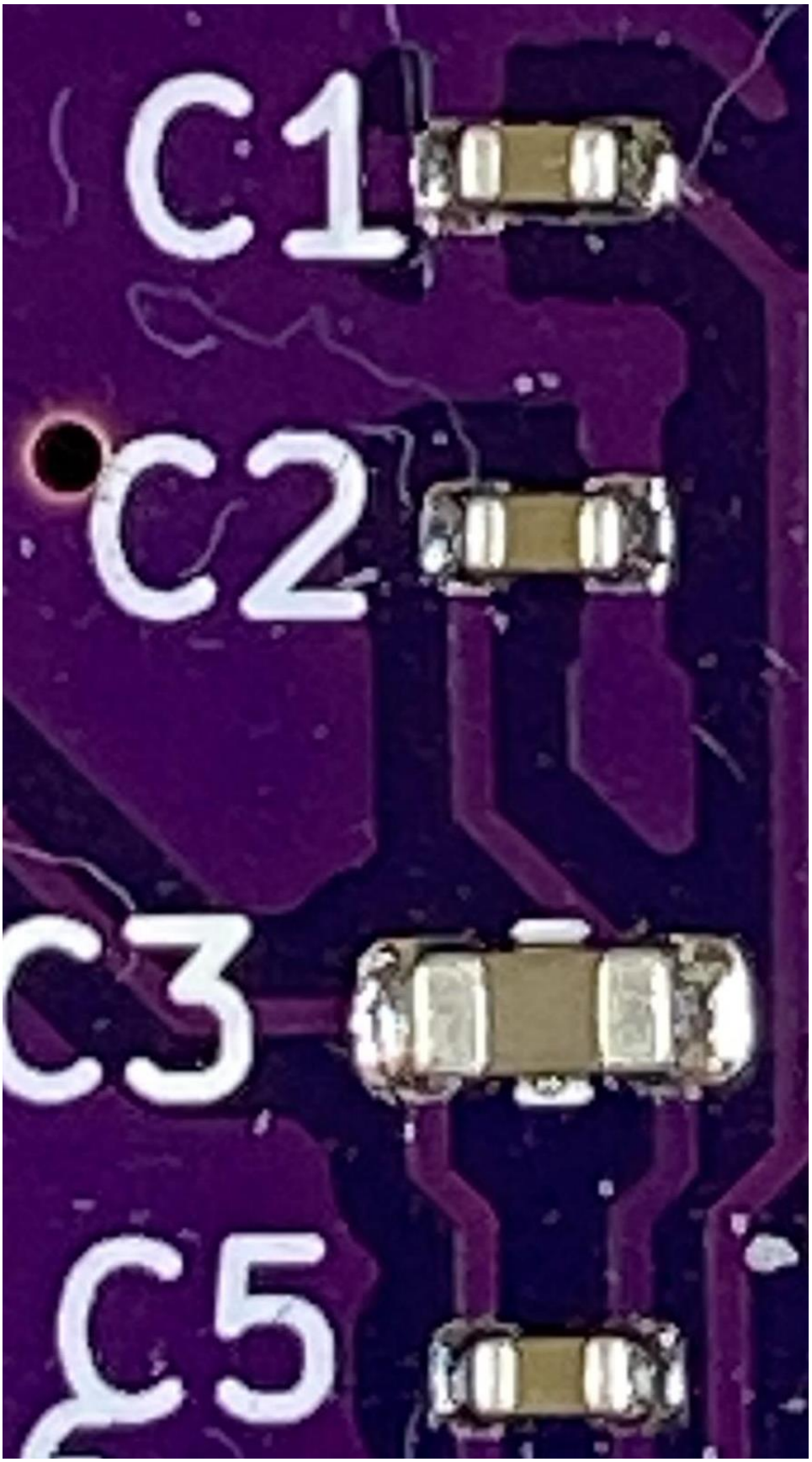



TEMP DISPLAY 1
TEMP DISPLAY 2
AIR
POWER

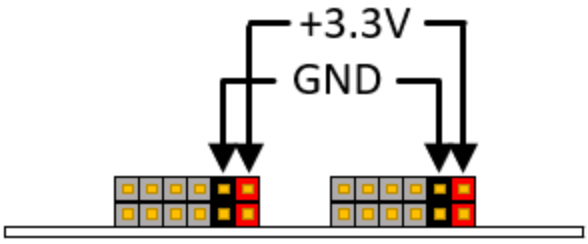



GND
±3.0V
1 KHz
+3.0V
-3.0V
SPI
PMOD B
PMOD C
Arty A7 Oscilloscope
Ledin Engineering, Inc.
Rev 3

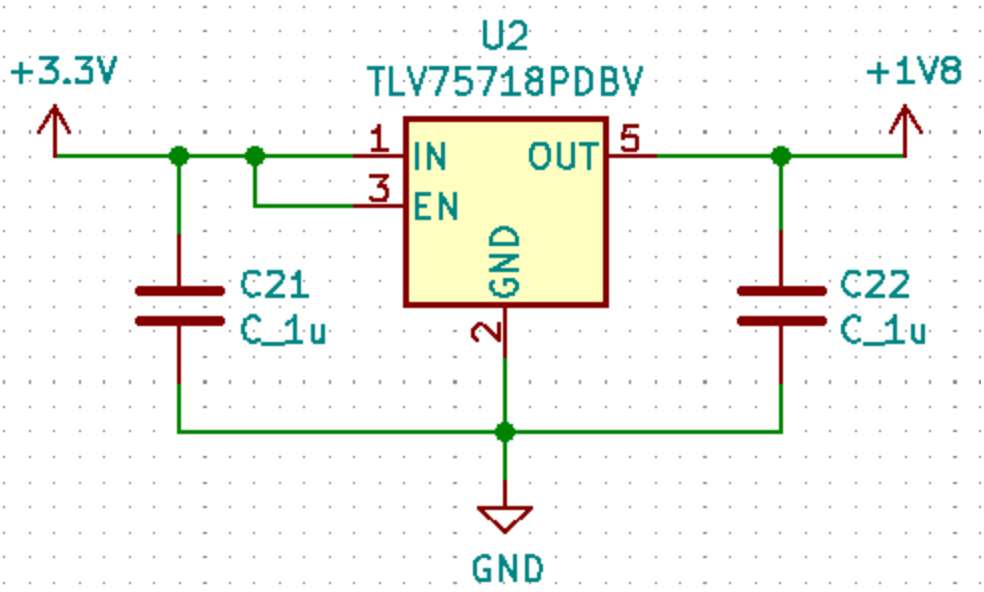

Reflow
T_L
Temperature
Soak
Preheat
Cooldown
Time

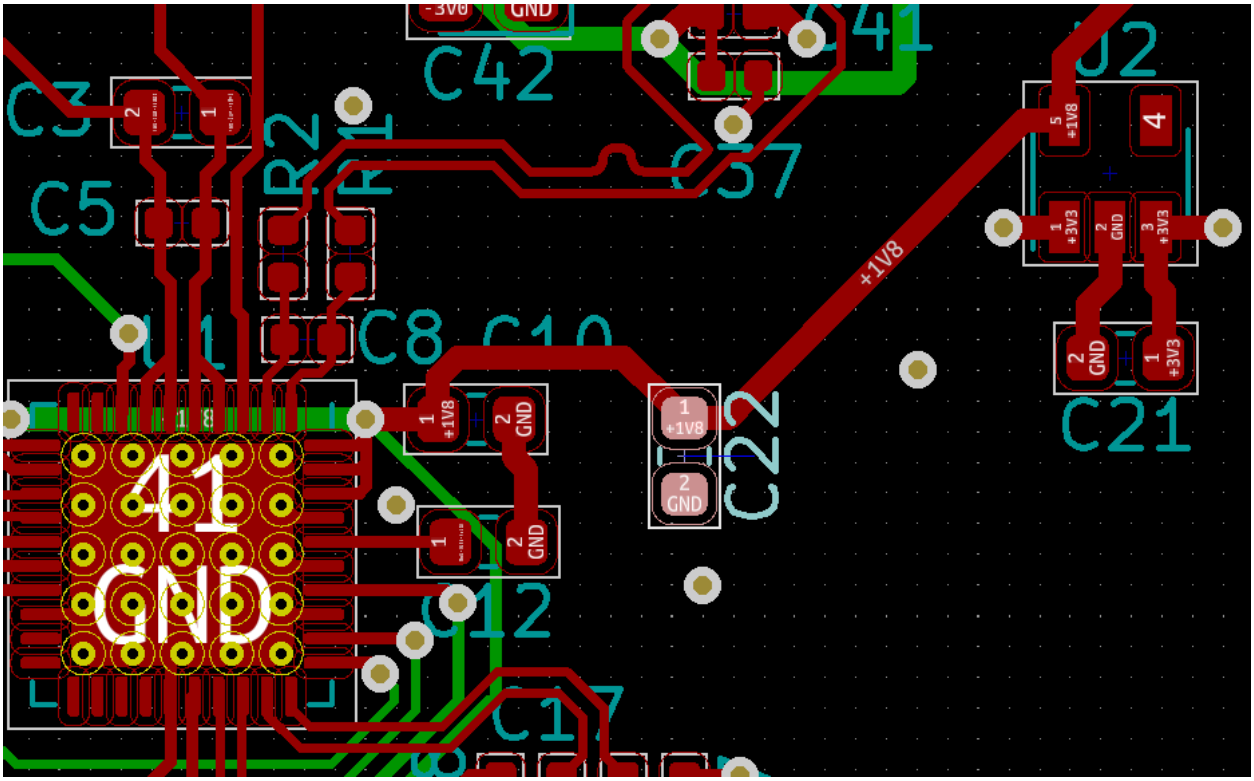

C1
C2
C3
C5

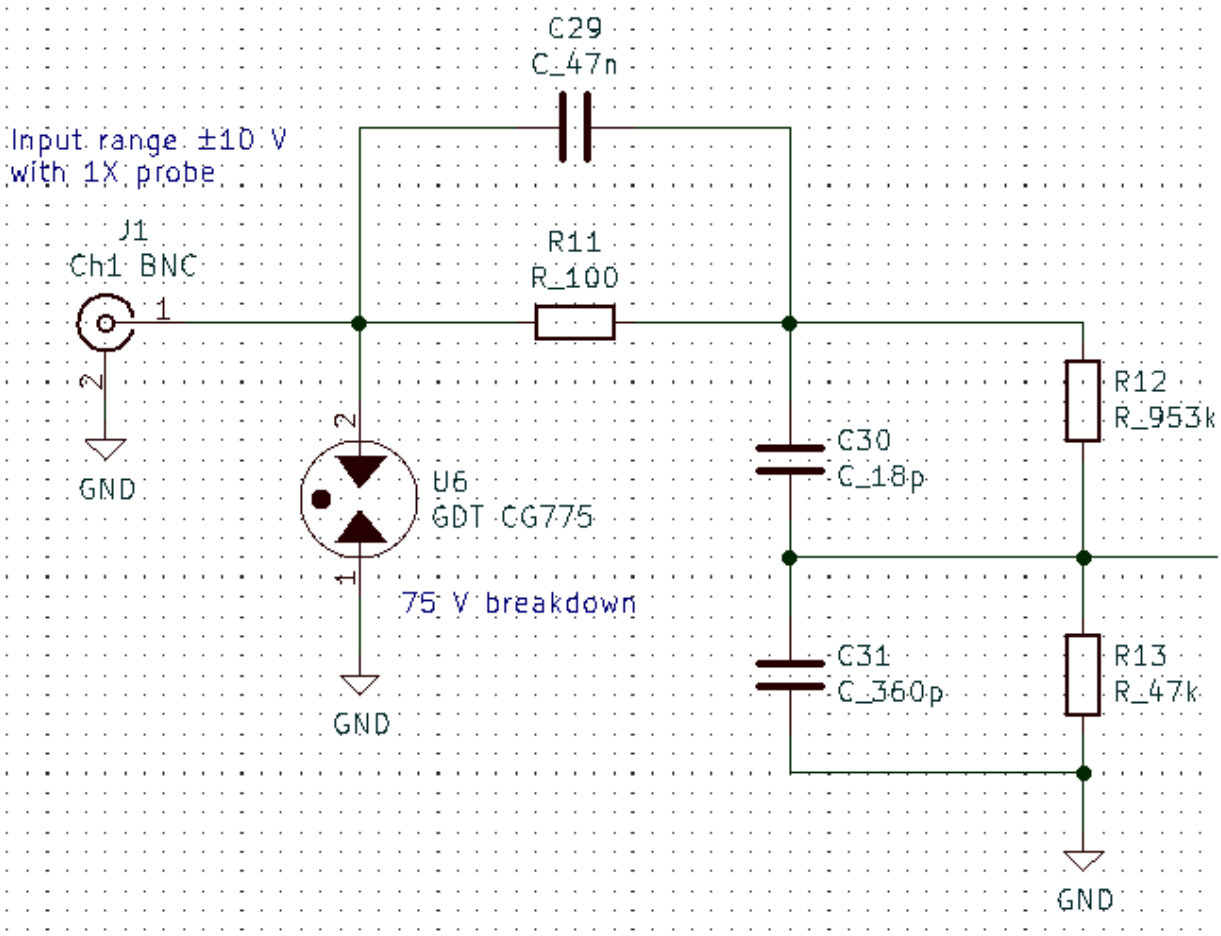

C1
C2
C3
C5

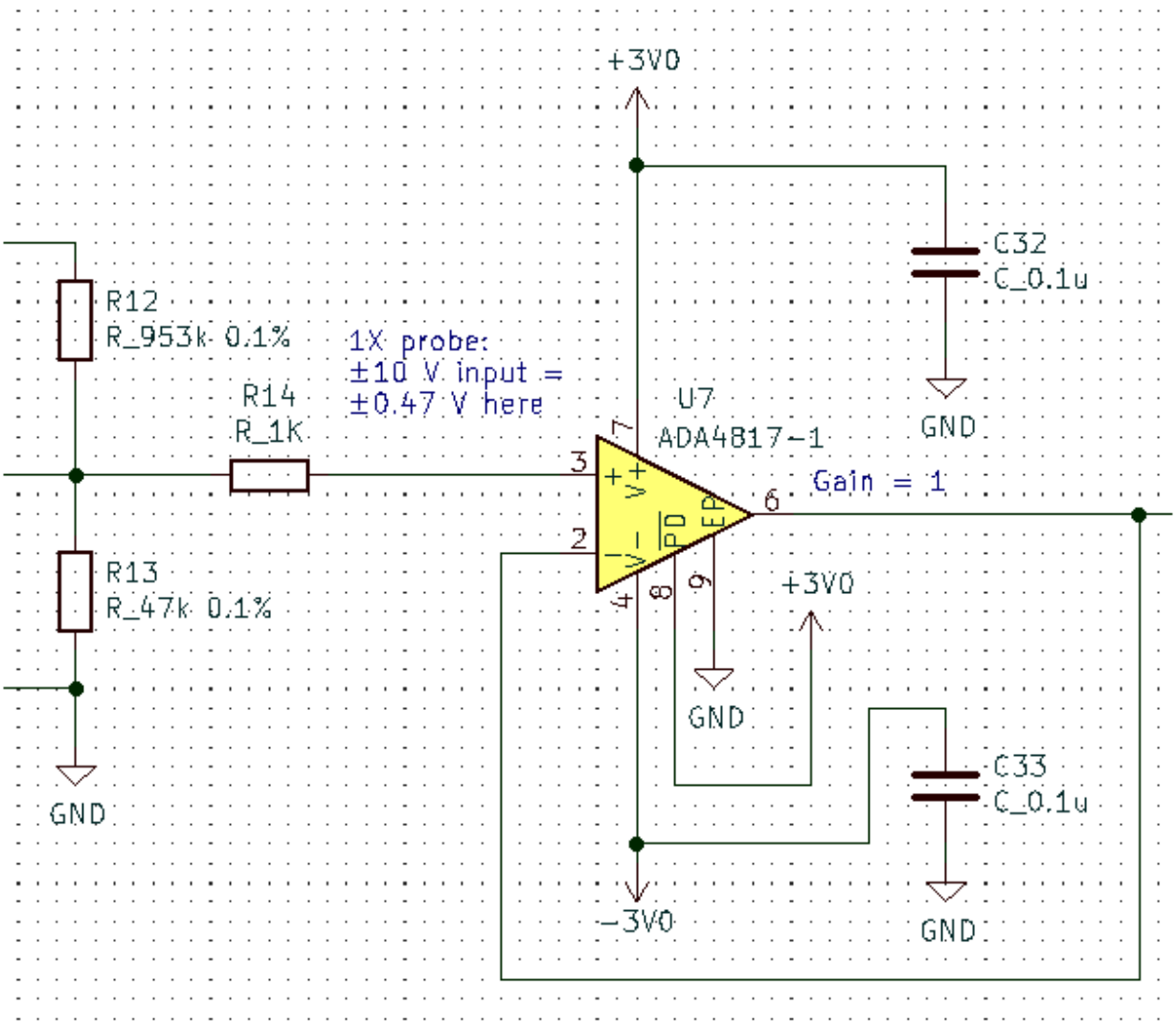

+3.3V
GND

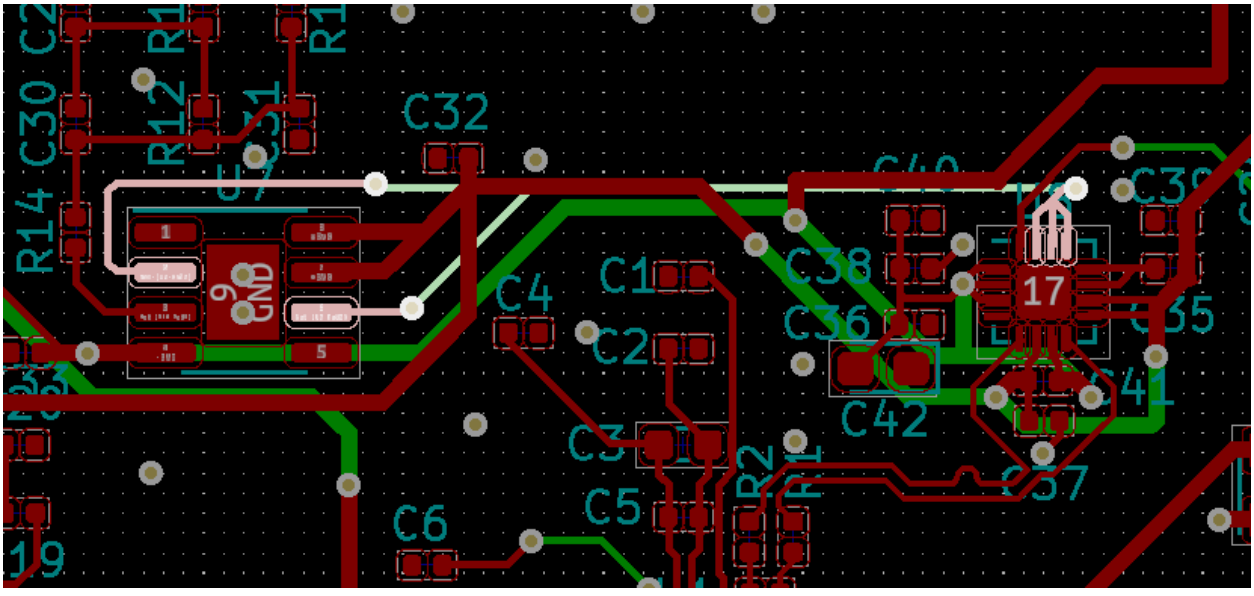
Chapter 8: Bringing Up the Board for the First Time

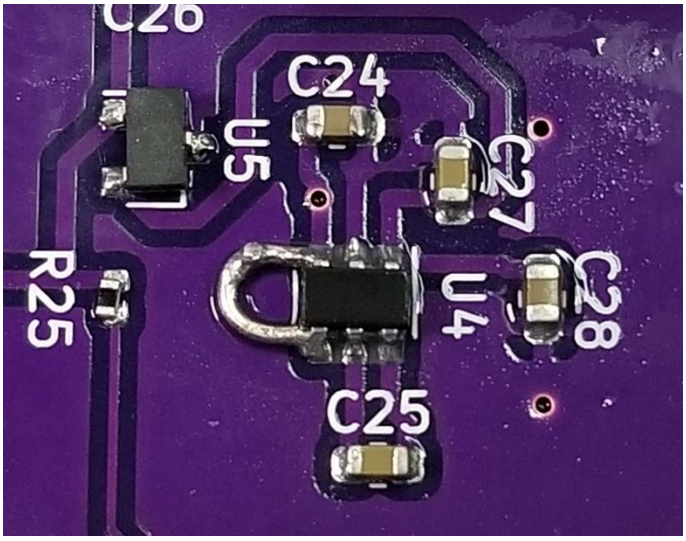


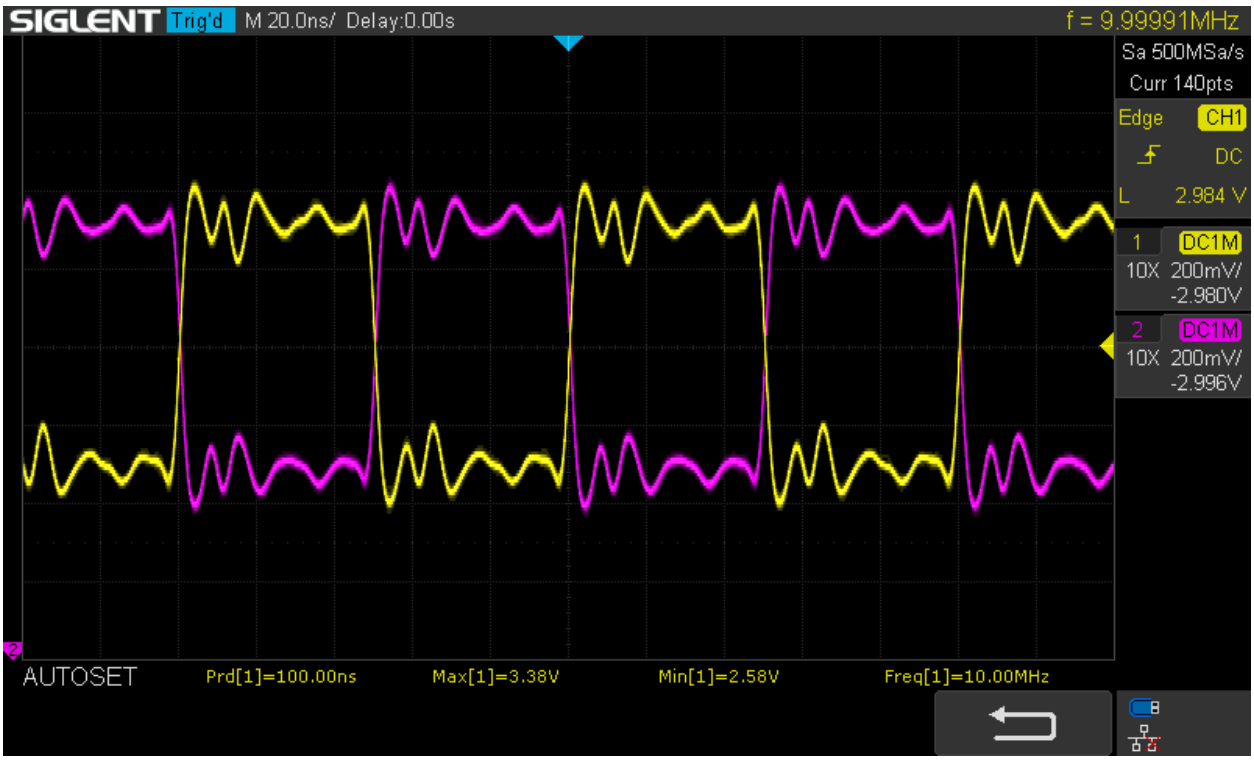

C42
C41
U2
C3
C5
R2
R1
C37
C8
C10
+1V8
C22
C21
41
GND
C12
C17

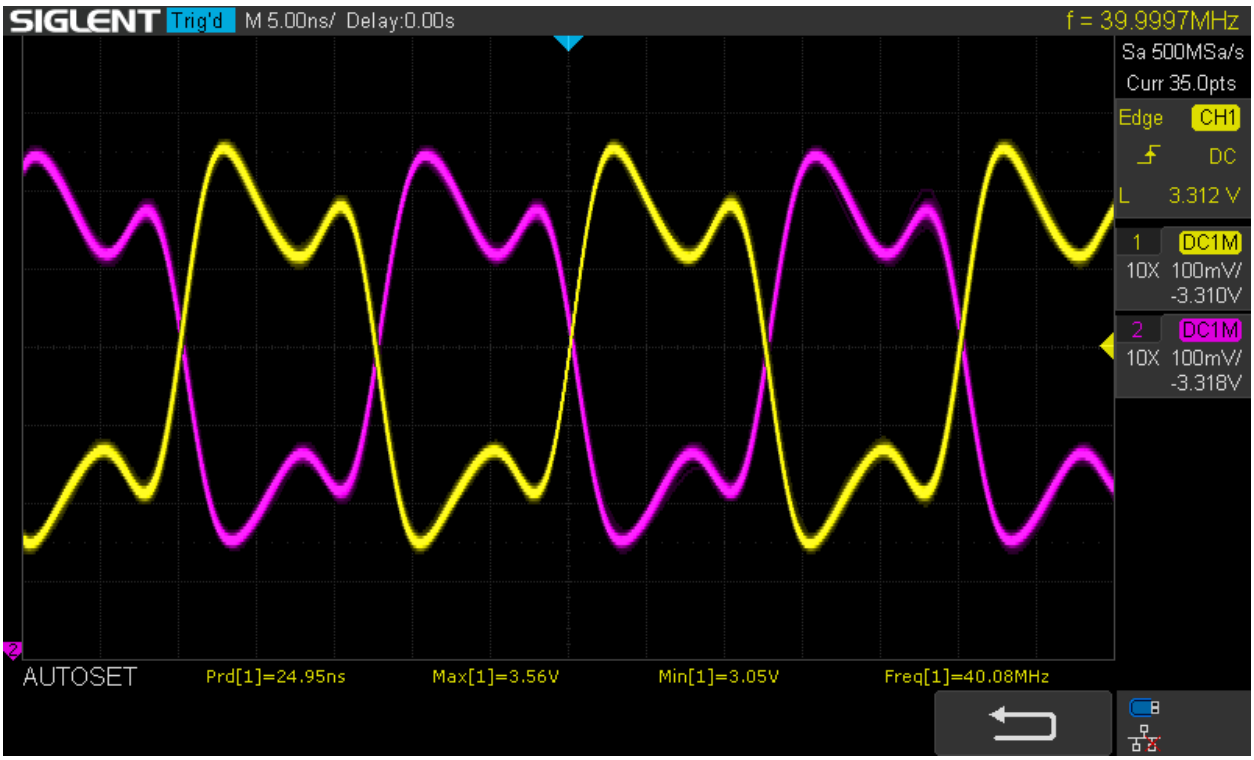

C29
C_47n
Input range ±10 V
with 1X probe
J1
Ch1 BNC
1
2
GND
R11
R_100
2
U6
GDT CG775
1
75 V breakdown
GND
C30
C_18p
C31
C_360p
R12
R_953k
R13
R_47k
GND


+3V0
C32
C_0.1u
GND
R12
R_953k 0.1%
1X probe:
±10 V input =
±0.47 V here
R14
R_1K
U7
ADA4817-1
Gain = 1
3
2
7
6
4
8
9
+3V0
R13
R_47k 0.1%
GND
GND
C33
C_0.1u
-3V0
GND

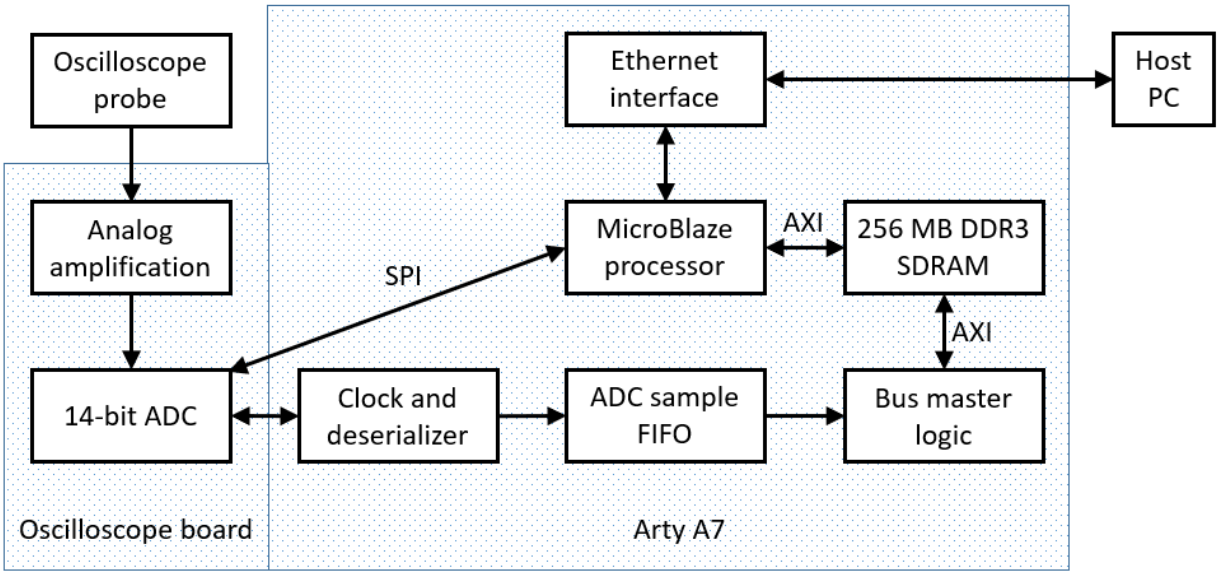

C32
C4
C1
C2
C3
C5
C6
C38
C36
C42
C41
C37
R2
R1
17
9
GND

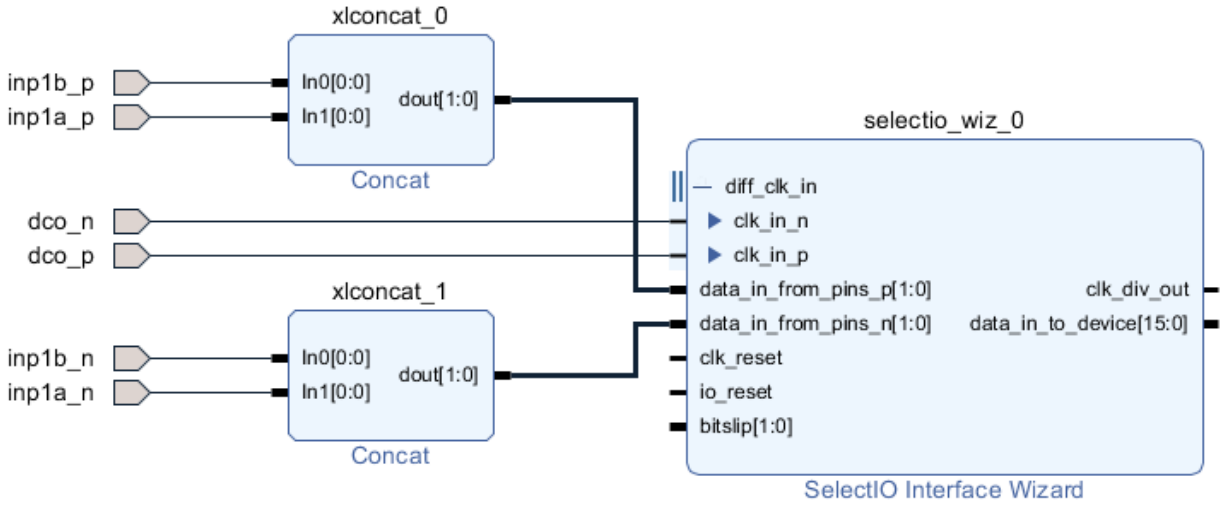

C26
C24
U5
C27
R25
U4
C28
C25

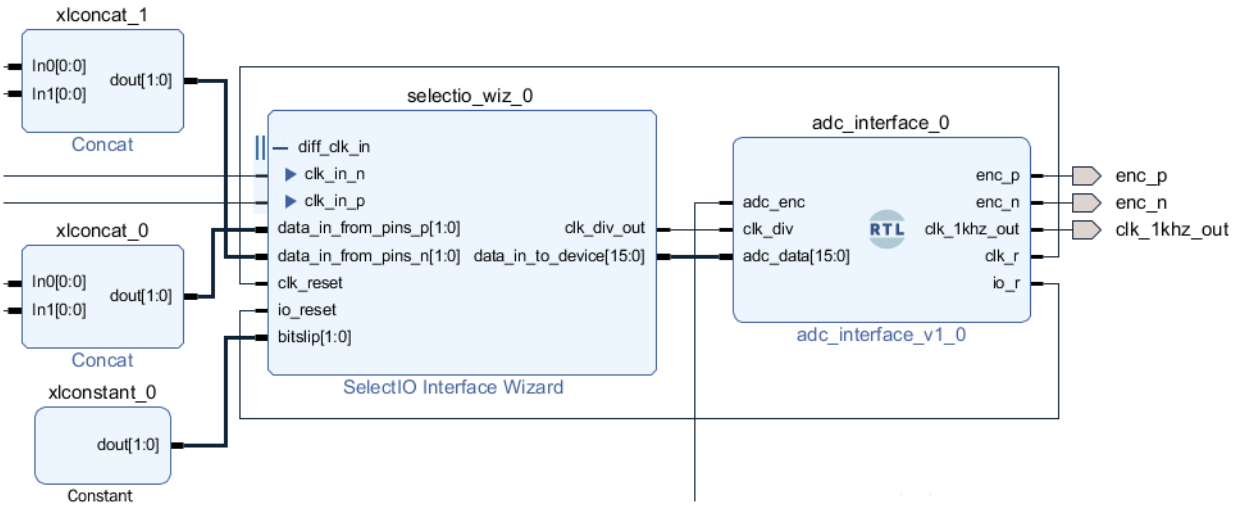

SIGLENT
Trig'd
M 20.0ns/ Delay:0.00s
f = 9.99991MHz
Sa 500MSa/s
Curr 140pts
Edge
CH1
DC
L 2.984 V
1 DC1M
10X 200mV/
-2.980V
2 DC1M
10X 200mV/
-2.996V
AUTOSET
Prd[1]=100.00ns
Max[1]=3.38V
Min[1]=2.58V
Freq[1]=10.00MHz

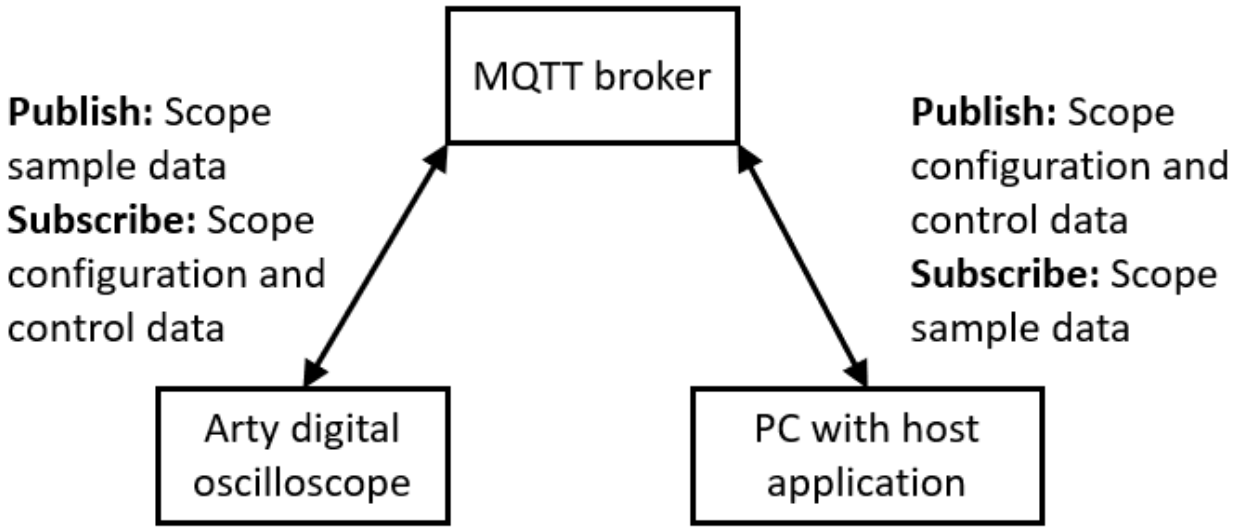

SIGLENT
Trig'd
M 5.00ns/ Delay:0.00s
f = 39.9997MHz
Sa 500MSa/s
Curr 35.0pts
Edge
CH1
DC
L 3.312 V
1 DC1M
10X 100mV/
-3.310V
2 DC1M
10X 100mV/
-3.318V
AUTOSET
Prd[1]=24.95ns
Max[1]=3.56V
Min[1]=3.05V
Freq[1]=40.08MHz

Chapter 9: The Firmware Development Process






xlconcat_1
In0[0:0]
In1[0:0]
dout[1:0]
Concat
xlconcat_0
In0[0:0]
In1[0:0]
dout[1:0]
Concat
xlconstant_0
dout[1:0]
Constant
selectio_wiz_0
diff_clk_in
clk_in_n
clk_in_p
data_in_from_pins_p[1:0]
data_in_from_pins_n[1:0]
clk_reset
io_reset
bitslip[1:0]
clk_div_out
data_in_to_device[15:0]
SelectIO Interface Wizard
adc_interface_0
adc_enc
clk_div
adc_data[15:0]
RTL
enc_p
enc_n
clk_1khz_out
clk_r
io_r
adc_interface_v1_0
enc_p
enc_n
clk_1khz_out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Arty digital oscilloscope
PC with host application

Chapter 10: Testing and Debugging the Embedded System