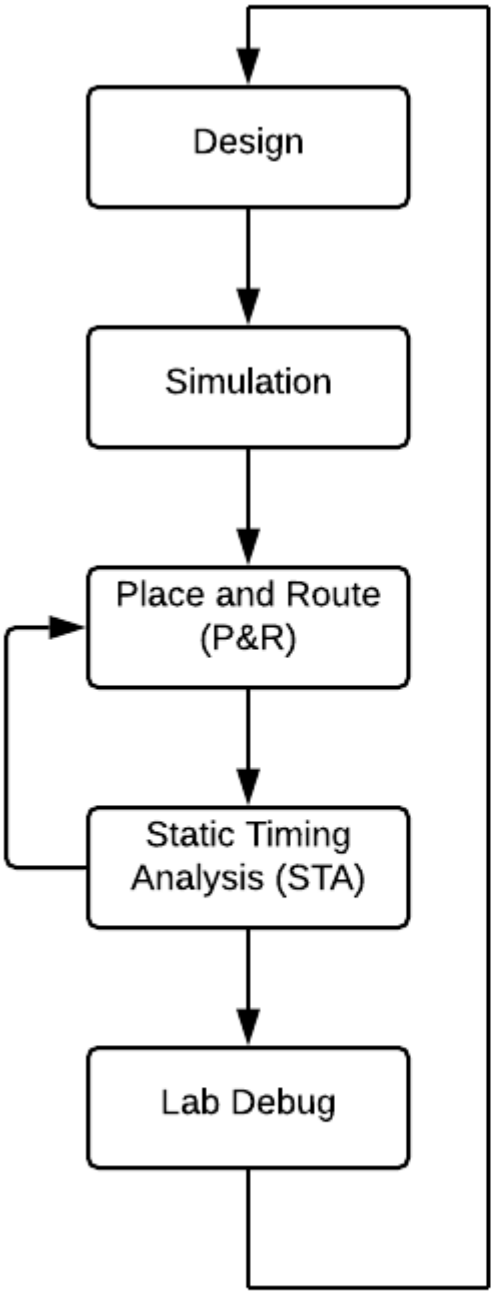
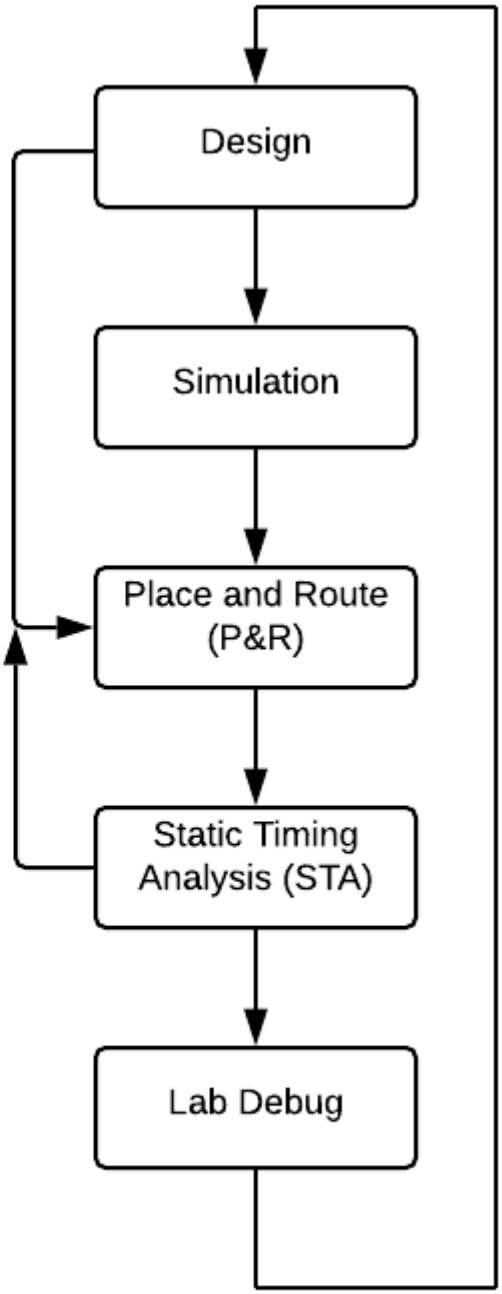
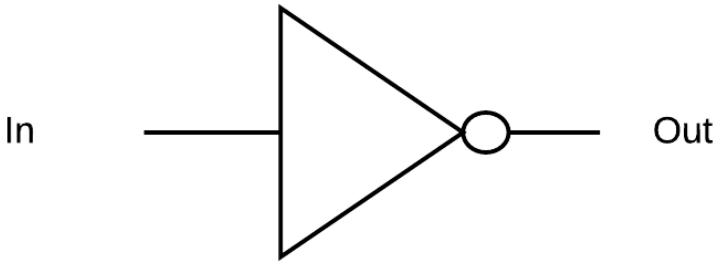
Chapter 1: Introduction to FPGA Architectures and Xilinx Vivado



Simple ASIC Flow



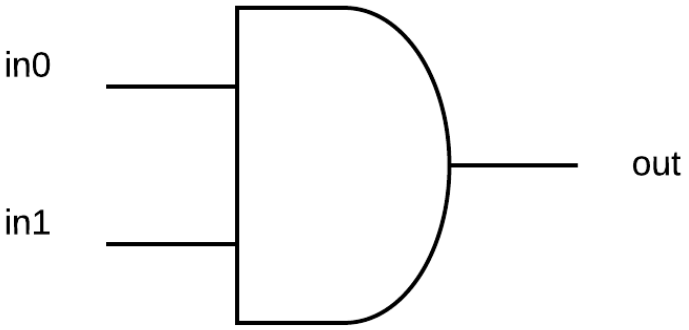
Simple FPGA Flow



Graphical Representation

In	Out
0	1
1	0

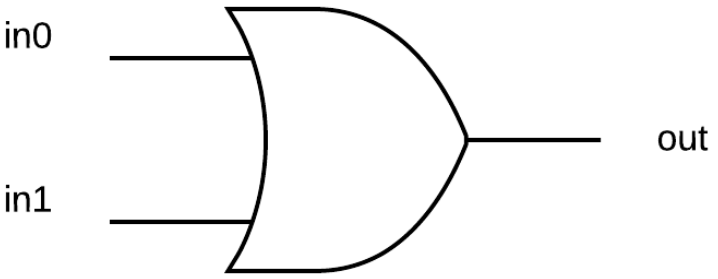
Truth Table



Graphical Representation

in0	in1	out
0	0	0
0	1	0
1	0	0
1	1	1

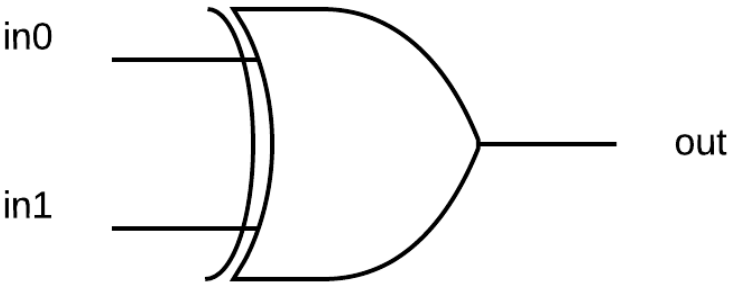
Truth Table



Graphical Representation

in0	in1	out
0	0	0
0	1	1
1	0	1
1	1	1

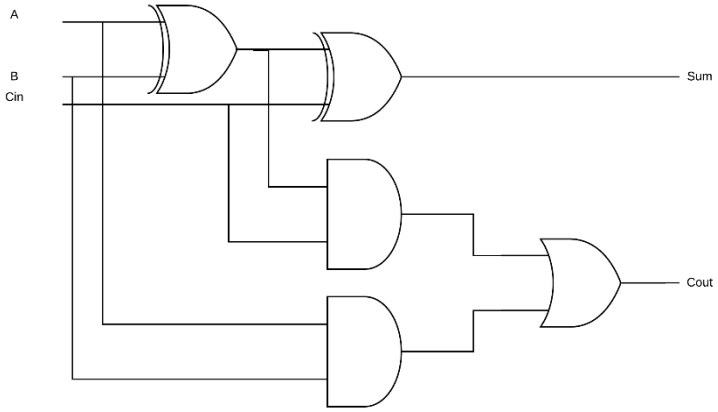
Truth Table



Graphical Representation

in0	in1	out
0	0	0
0	1	1
1	0	1
1	1	0

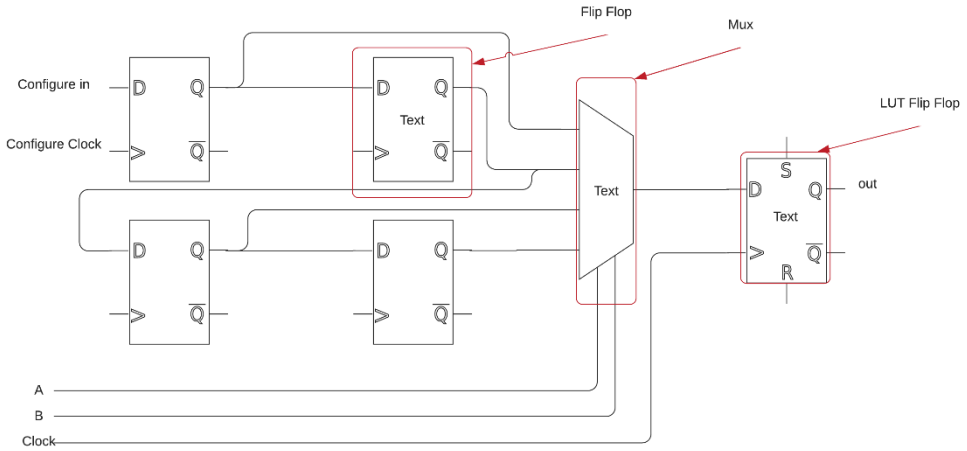
Truth Table

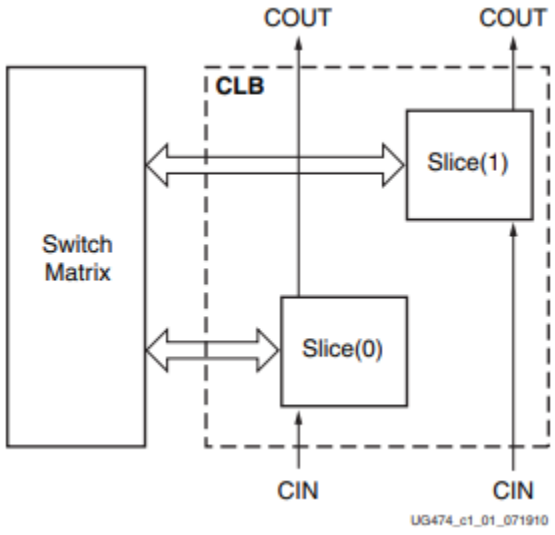


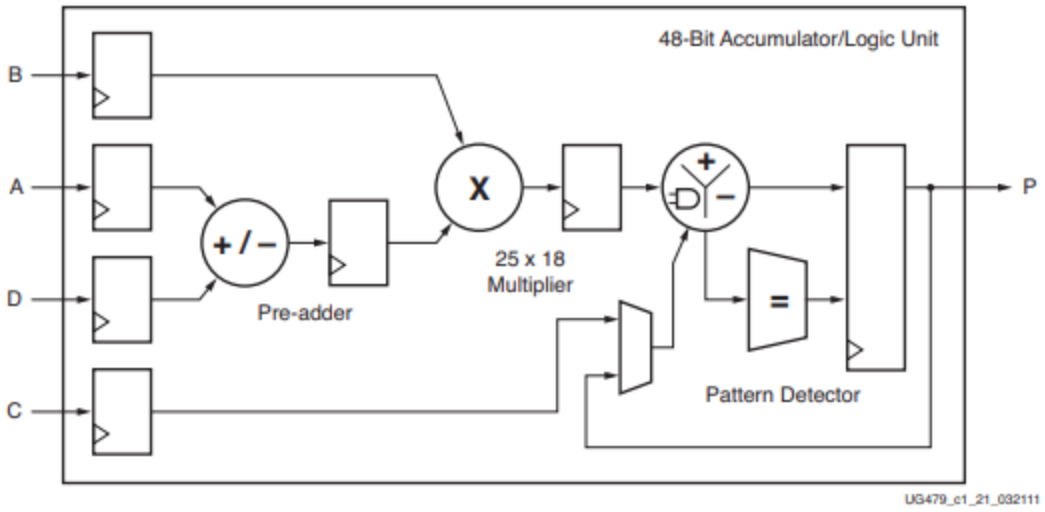
Graphical Representation

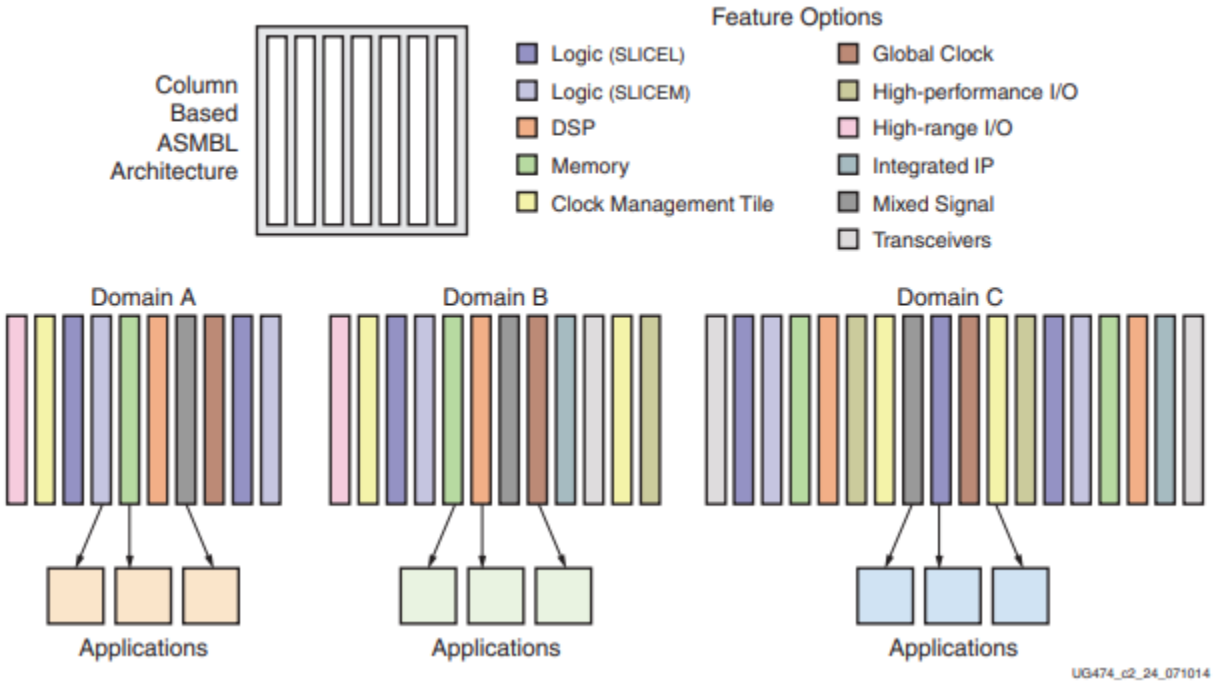
A	B	Cin	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

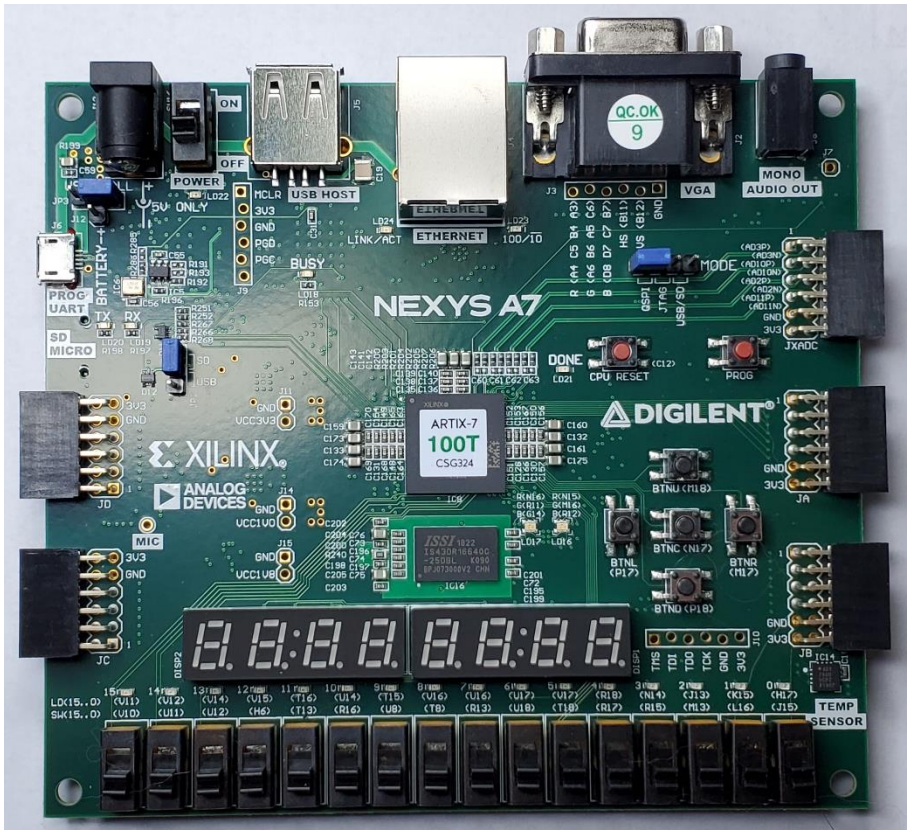
Truth Table

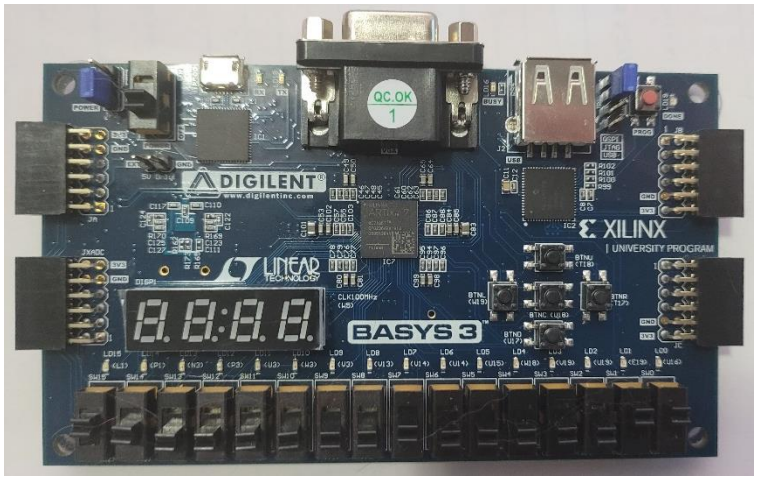


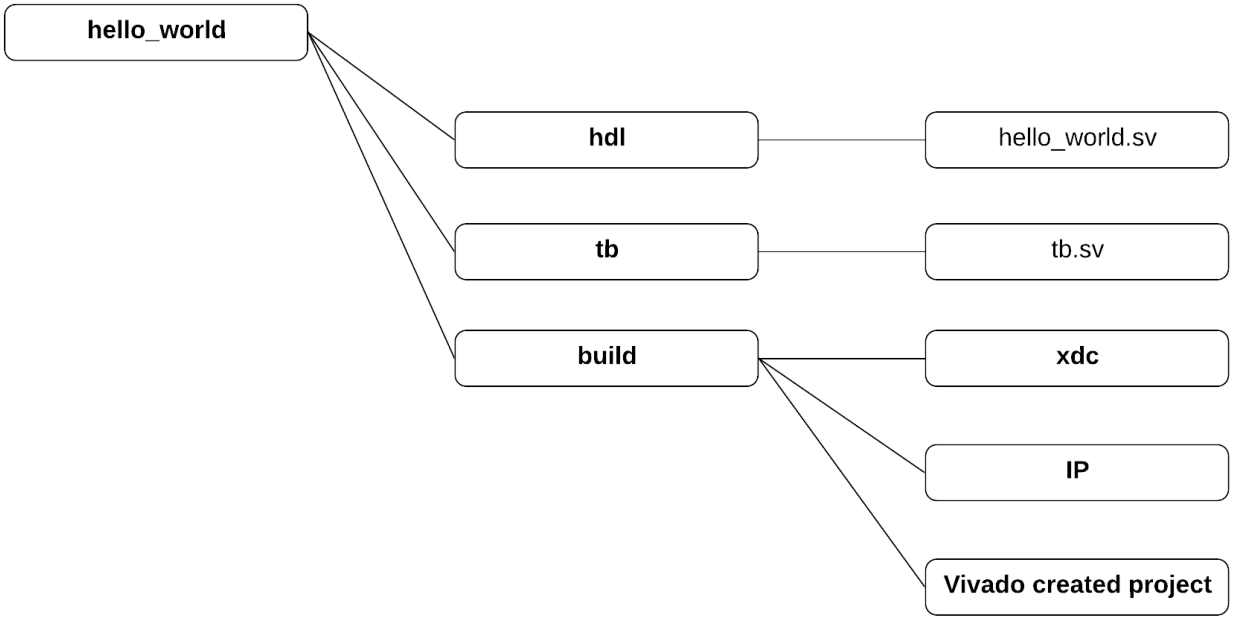


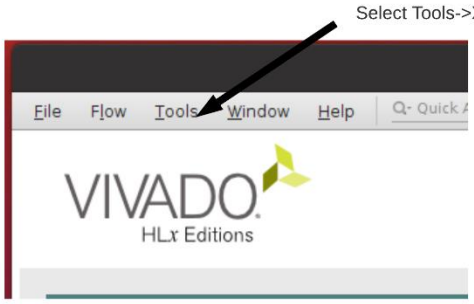

48-Bit Accumulator/Logic Unit
B
A
D
C
+ / –
Pre-adder
X
25 x 18
Multiplier
+
D
–
=
Pattern Detector
P
UG479_c1_21_032111

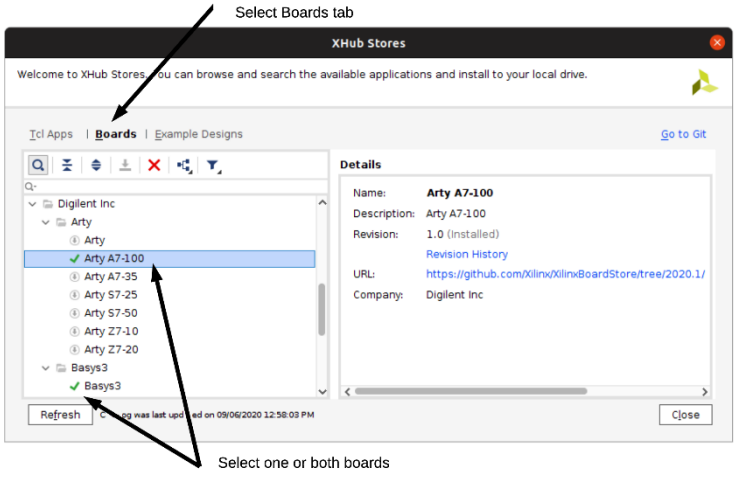

Column
Based
ASMBL
Architecture
Feature Options
Logic (SLICEL)
Logic (SLICEM)
DSP
Memory
Clock Management Tile
Global Clock
High-performance I/O
High-range I/O
Integrated IP
Mixed Signal
Transceivers
Domain A
Domain B
Domain C
Applications
Applications
Applications
UG474_c2_24_071014

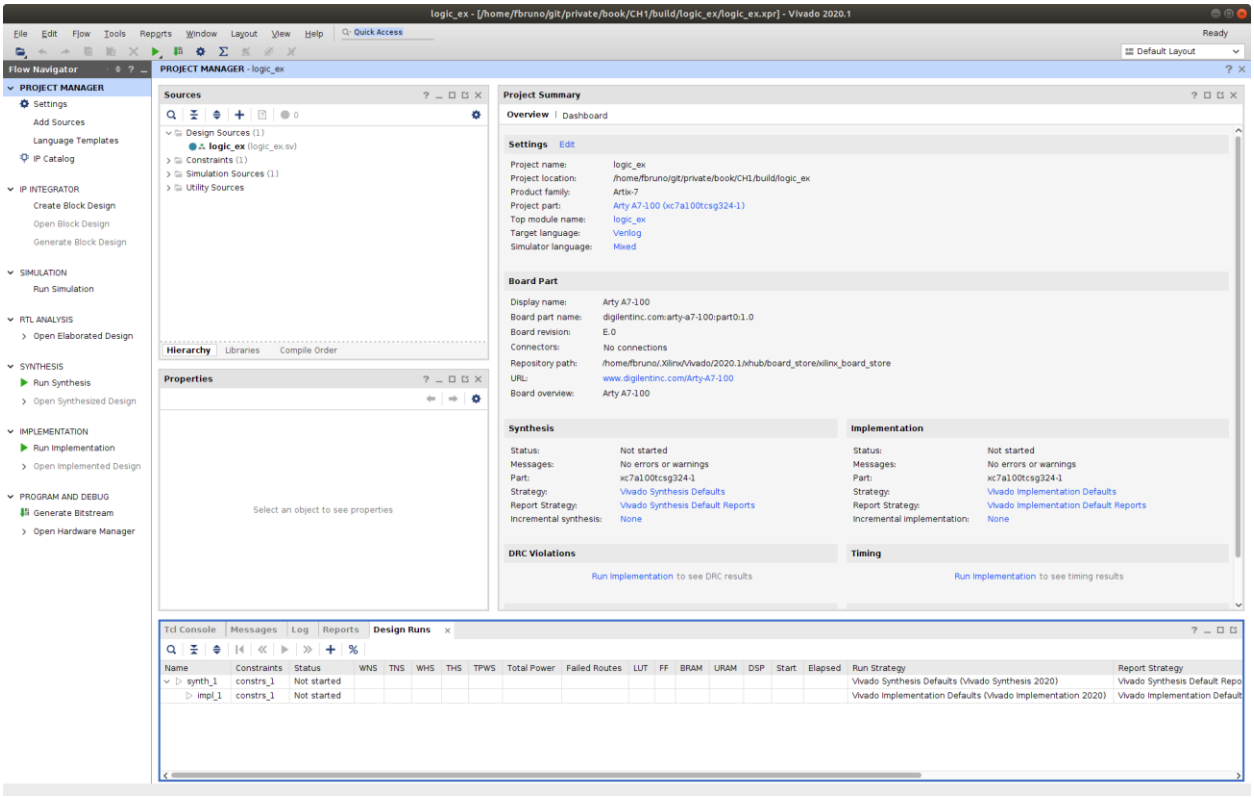

NEXYS A7
DIGILENT
XILINX
ARTIX-7
100T
CSG324
QC.OK
9
POWER
ON
OFF
USB HOST
ETHERNET
VGA
MONO
AUDIO OUT
PROG
UART
SD
MICRO
MODE
CPU RESET
PROG
JXADC
BTNU (M18)
BTNC (N17)
BTNL (P17)
BTNR (M17)
BTND (P18)
MIC
TEMP
SENSOR

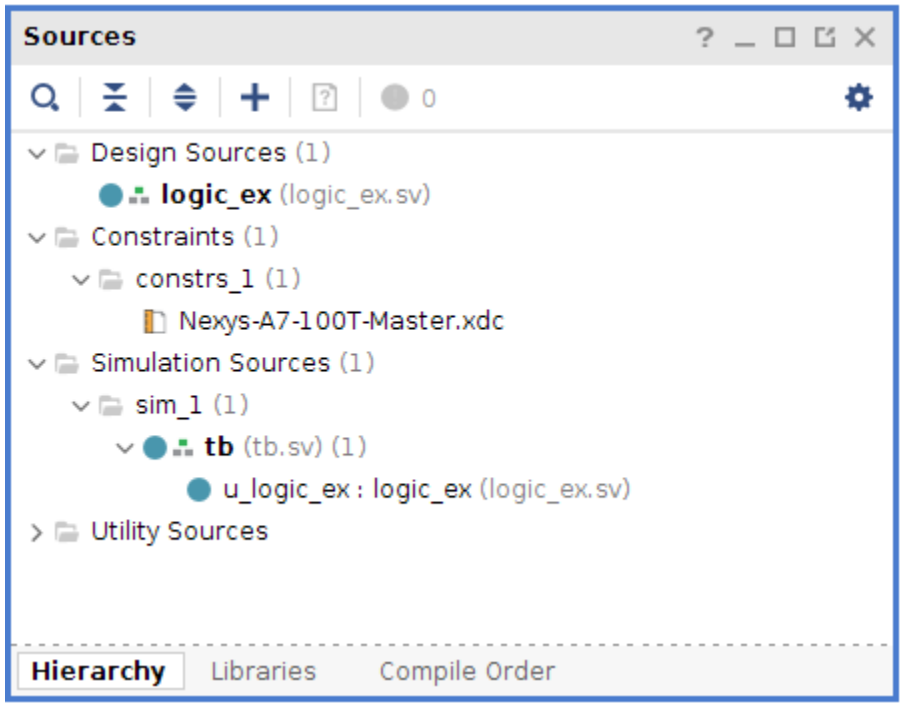

QC.OK
1
DIGILENT
XILINX
UNIVERSITY PROGRAM
LINEAR TECHNOLOGY
BASYS 3

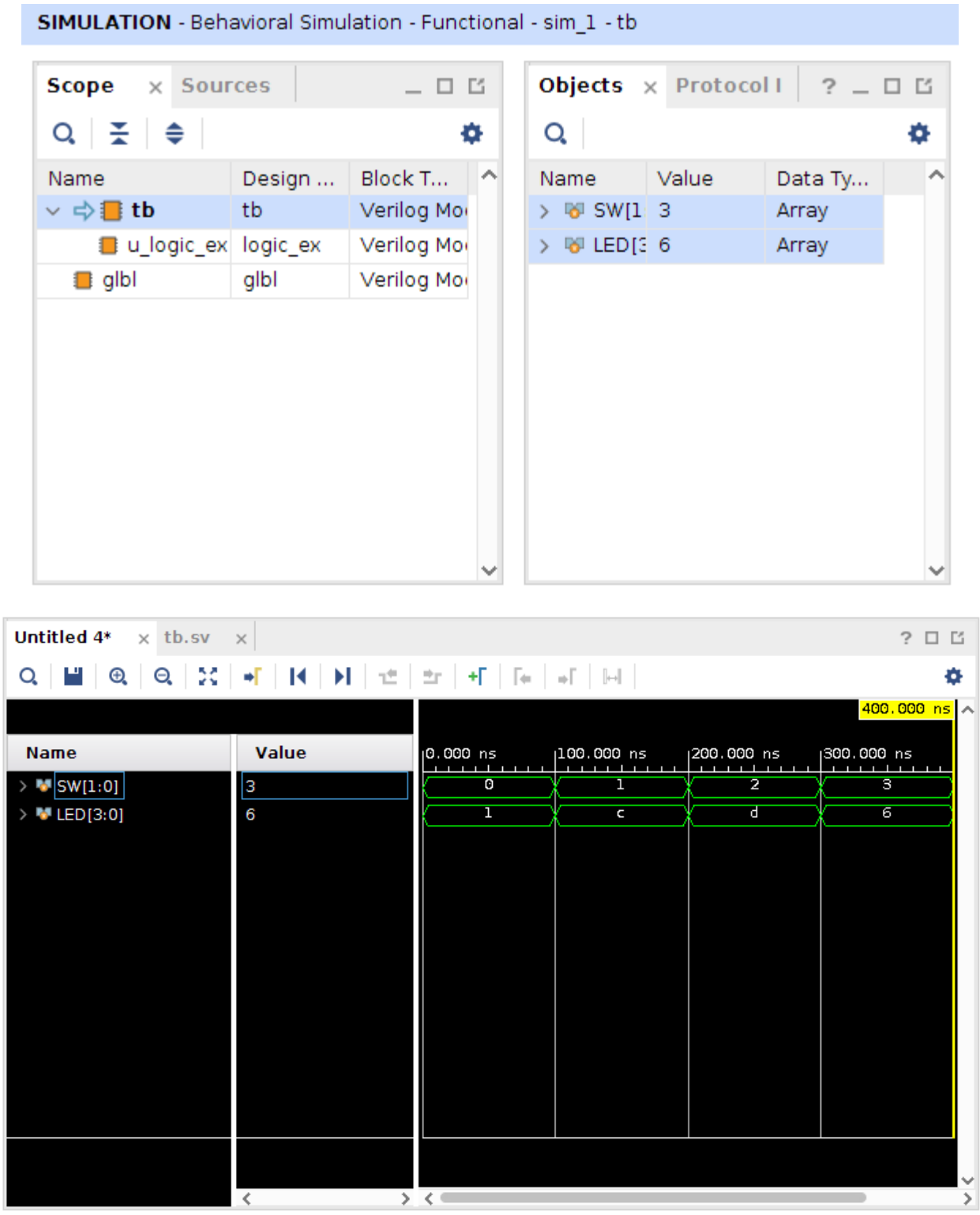

hello_world
hdl
hello_world.sv
tb
tb.sv
build
xdc
IP
Vivado created project

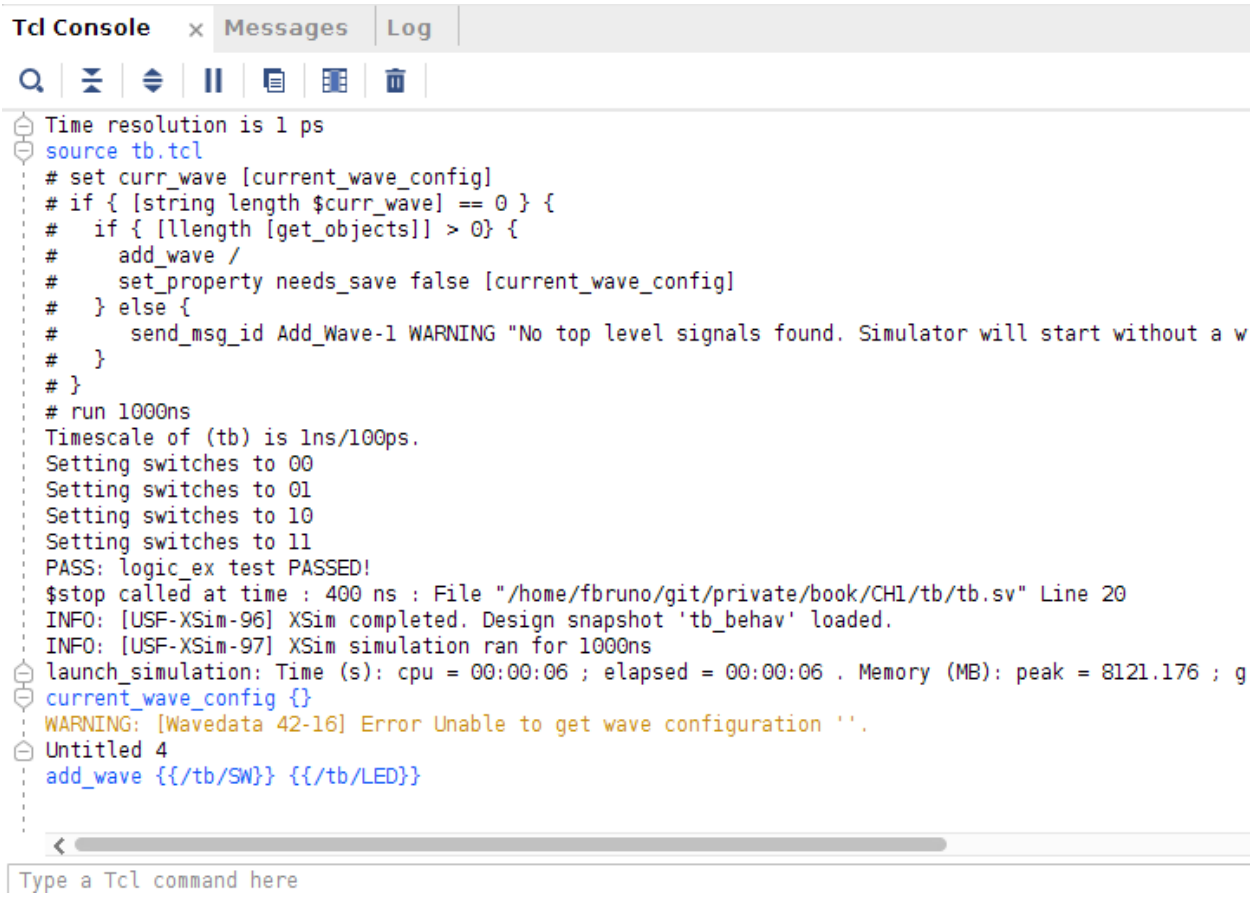

Select Tools->Xhub Stores
File
Flow
Tools
Window
Help
VIVADO
HLx Editions

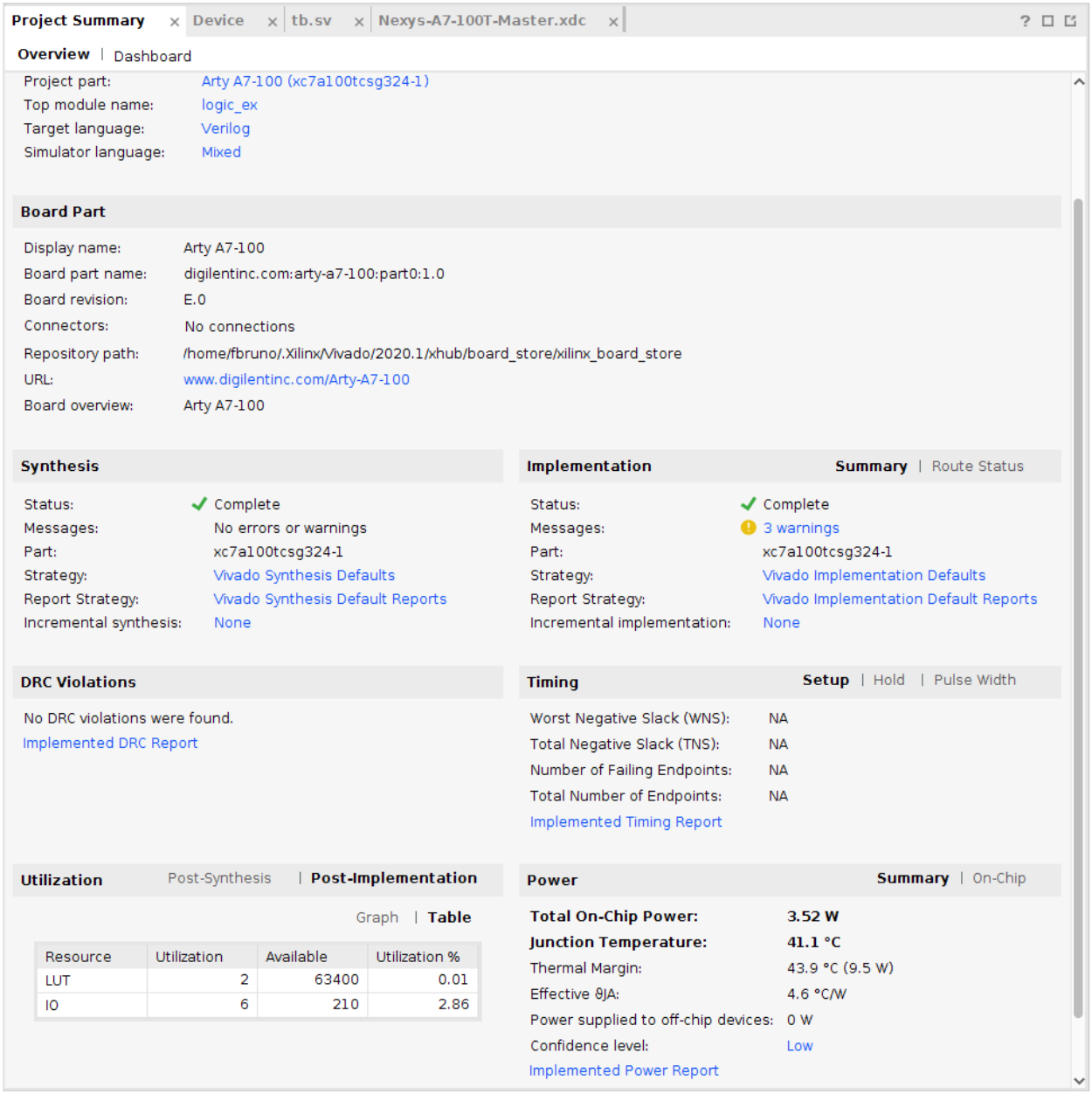

Select Boards tab
XHub Stores
Welcome to XHub Stores. You can browse and search the available applications and install to your local drive.
Tcl Apps
Boards
Example Designs
Go to Git
Digilent Inc
Arty
Arty
Arty A7-100
Arty A7-35
Arty S7-25
Arty S7-50
Arty Z7-10
Arty Z7-20
Basys3
Basys3
Details
Name: Arty A7-100
Description: Arty A7-100
Revision: 1.0 (Installed)
Revision History
URL: https://github.com/Xilinx/XilinxBoardStore/tree/2020.1/
Company: Digilent Inc
Refresh
Close
Select one or both boards

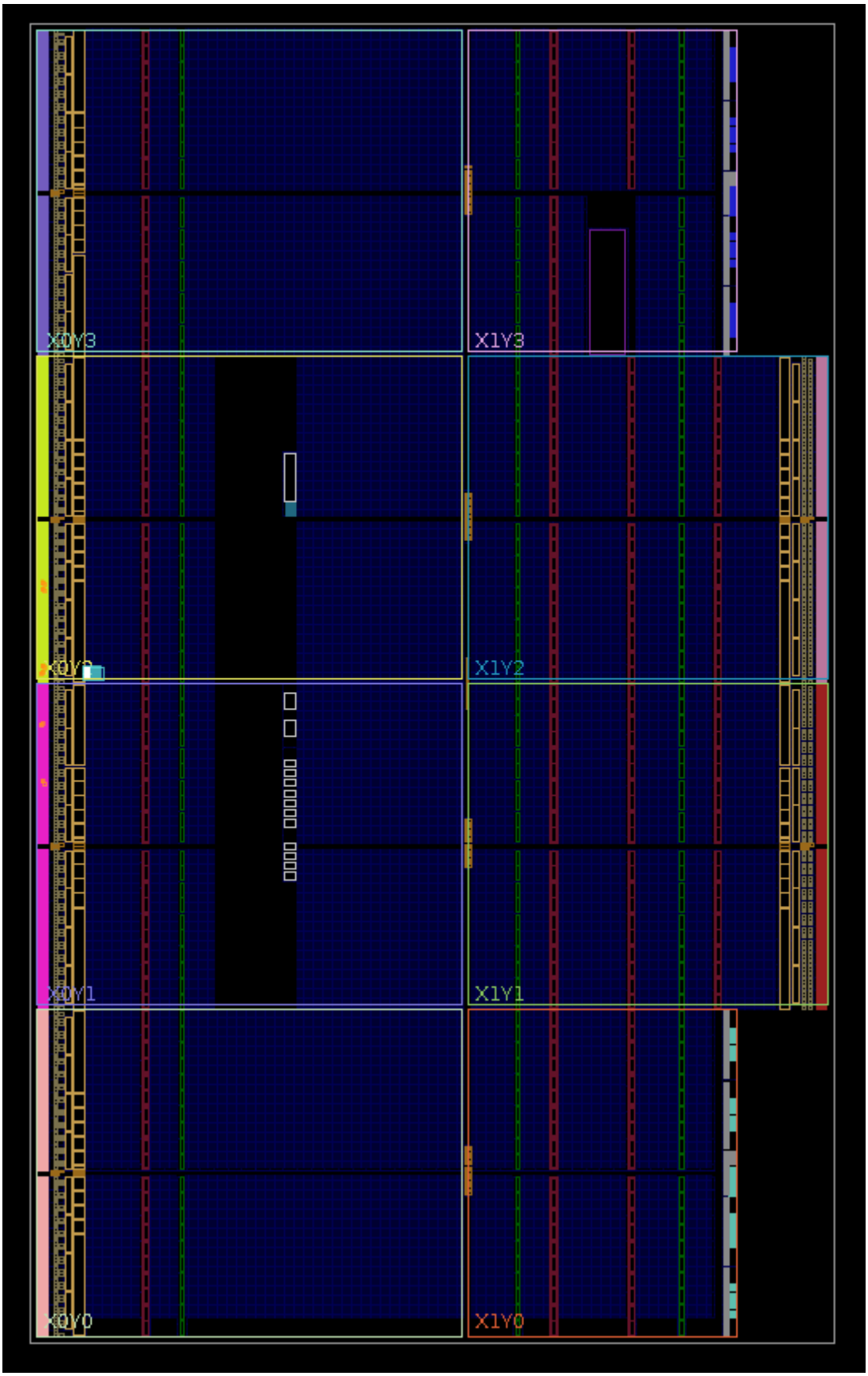

logic_ex - [/home/fbruno/git/private/book/CH1/build/logic_ex/logic_ex.xpr] - Vivado 2020.1
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Ready
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
PROJECT MANAGER - logic_ex
Sources
Design Sources (1)
logic_ex (logic_ex.sv)
Constraints (1)
Simulation Sources (1)
Utility Sources
Hierarchy Libraries Compile Order
Properties
Select an object to see properties
Project Summary
Overview | Dashboard
Settings Edit
Project name: logic_ex
Project location: /home/fbruno/git/private/book/CH1/build/logic_ex
Product family: Artix-7
Project part: Arty A7-100 (xc7a100tcsg324-1)
Top module name: logic_ex
Target language: Verilog
Simulator language: Mixed
Board Part
Display name: Arty A7-100
Board part name: digilentinc.com:arty-a7-100:part0:1.0
Board revision: E.0
Connectors: No connections
Repository path: /home/fbruno/.Xilinx/Vivado/2020.1/xhub/board_store/xilinx_board_store
URL: www.digilentinc.com/Arty-A7-100
Board overview: Arty A7-100
Synthesis
Status: Not started
Messages: No errors or warnings
Part: xc7a100tcsg324-1
Strategy: Vivado Synthesis Defaults
Report Strategy: Vivado Synthesis Default Reports
Incremental synthesis: None
Implementation
Status: Not started
Messages: No errors or warnings
Part: xc7a100tcsg324-1
Strategy: Vivado Implementation Defaults
Report Strategy: Vivado Implementation Default Reports
Incremental implementation: None
DRC Violations
Run Implementation to see DRC results
Timing
Run Implementation to see timing results
Tcl Console Messages Log Reports Design Runs
Name Constraints Status WNS TNS WHS THS TPWS Total Power Failed Routes LUT FF BRAM URAM DSP Start Elapsed Run Strategy Report Strategy
synth_1 constrs_1 Not started Vivado Synthesis Defaults (Vivado Synthesis 2020) Vivado Synthesis Default Repo
impl_1 constrs_1 Not started Vivado Implementation Defaults (Vivado Implementation 2020) Vivado Implementation Default

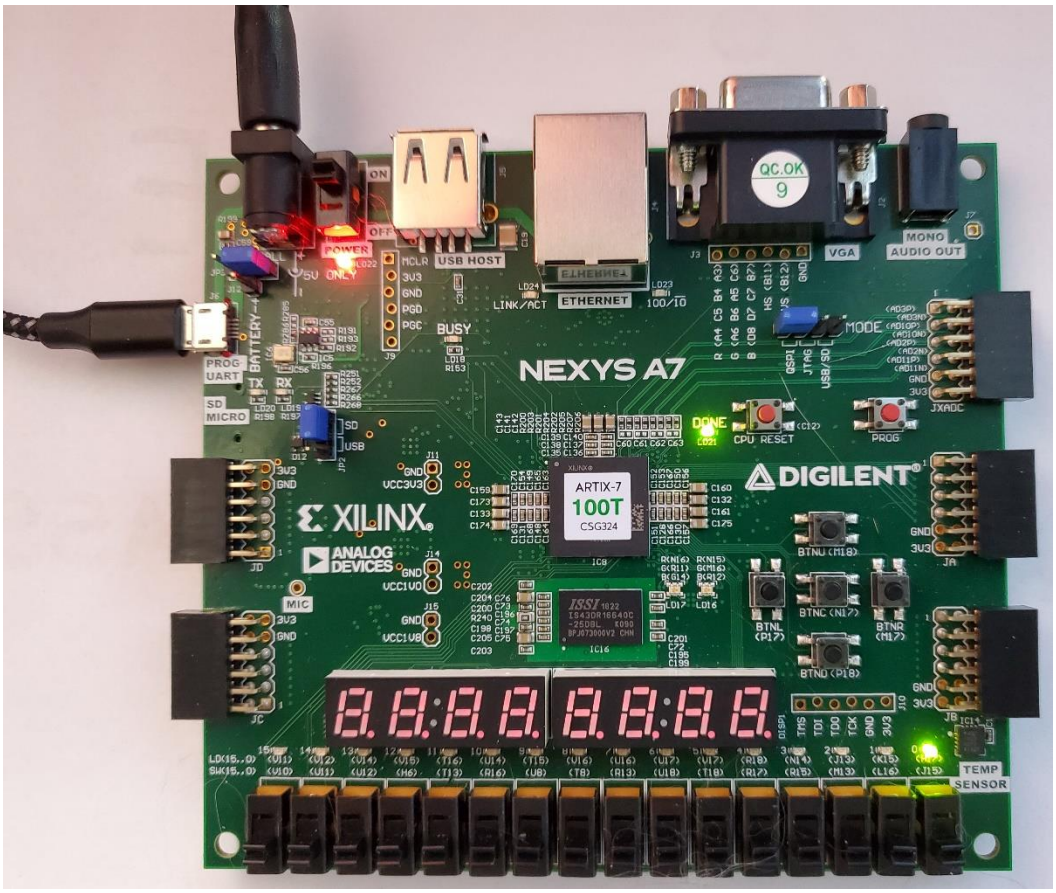

Sources
0
Design Sources (1)
logic_ex (logic_ex.sv)
Constraints (1)
constrs_1 (1)
Nexys-A7-100T-Master.xdc
Simulation Sources (1)
sim_1 (1)
tb (tb.sv) (1)
u_logic_ex : logic_ex (logic_ex.sv)
Utility Sources
Hierarchy
Libraries
Compile Order


SIMULATION - Behavioral Simulation - Functional - sim_1 - tb
Scope
Sources
Name
Design ...
Block T...
tb
tb
Verilog Mo
u_logic_ex
logic_ex
Verilog Mo
glbl
glbl
Verilog Mo
Objects
Protocol I
Name
Value
Data Ty...
SW[1
3
Array
LED[3
6
Array
Untitled 4*
tb.sv
Name
Value
SW[1:0]
3
LED[3:0]
6
400.000 ns
0.000 ns
100.000 ns
200.000 ns
300.000 ns
0
1
2
3
1
c
d
6

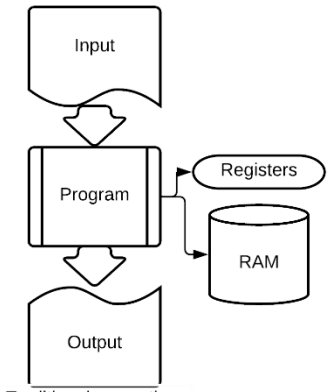

Tcl Console
Messages
Log
Time resolution is 1 ps
source tb.tcl
set curr_wave [current_wave_config]
if { [string length $curr_wave] == 0 } {
if { [llength [get_objects]] > 0} {
add_wave /
set_property needs_save false [current_wave_config]
} else {
send_msg_id Add_Wave-1 WARNING "No top level signals found. Simulator will start without a w
}
}
run 1000ns
Timescale of (tb) is 1ns/100ps.
Setting switches to 00
Setting switches to 01
Setting switches to 10
Setting switches to 11
PASS: logic_ex test PASSED!
$stop called at time : 400 ns : File "/home/fbruno/git/private/book/CH1/tb/tb.sv" Line 20
INFO: [USF-XSim-96] XSim completed. Design snapshot 'tb_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:06 ; elapsed = 00:00:06 . Memory (MB): peak = 8121.176 ; g
current_wave_config {}
WARNING: [Wavedata 42-16] Error Unable to get wave configuration ''.
Untitled 4
add_wave {{/tb/SW}} {{/tb/LED}}
Type a Tcl command here


Project Summary
Device
tb.sv
Nexys-A7-100T-Master.xdc
Overview | Dashboard
Project part: Arty A7-100 (xc7a100tcsg324-1)
Top module name: logic_ex
Target language: Verilog
Simulator language: Mixed
Board Part
Display name: Arty A7-100
Board part name: digilentinc.com:arty-a7-100:part0:1.0
Board revision: E.0
Connectors: No connections
Repository path: /home/fbruno/.Xilinx/Vivado/2020.1/xhub/board_store/xilinx_board_store
URL: www.digilentinc.com/Arty-A7-100
Board overview: Arty A7-100
Synthesis
Status: Complete
Messages: No errors or warnings
Part: xc7a100tcsg324-1
Strategy: Vivado Synthesis Defaults
Report Strategy: Vivado Synthesis Default Reports
Incremental synthesis: None
Implementation
Summary | Route Status
Status: Complete
Messages: 3 warnings
Part: xc7a100tcsg324-1
Strategy: Vivado Implementation Defaults
Report Strategy: Vivado Implementation Default Reports
Incremental implementation: None
DRC Violations
No DRC violations were found.
Implemented DRC Report
Timing
Setup | Hold | Pulse Width
Worst Negative Slack (WNS): NA
Total Negative Slack (TNS): NA
Number of Failing Endpoints: NA
Total Number of Endpoints: NA
Implemented Timing Report
Utilization
Post-Synthesis | Post-Implementation
Graph | Table
Resource Utilization Available Utilization %
LUT 2 63400 0.01
IO 6 210 2.86
Power
Summary | On-Chip
Total On-Chip Power: 3.52 W
Junction Temperature: 41.1 °C
Thermal Margin: 43.9 °C (9.5 W)
Effective ϑJA: 4.6 °C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
Implemented Power Report

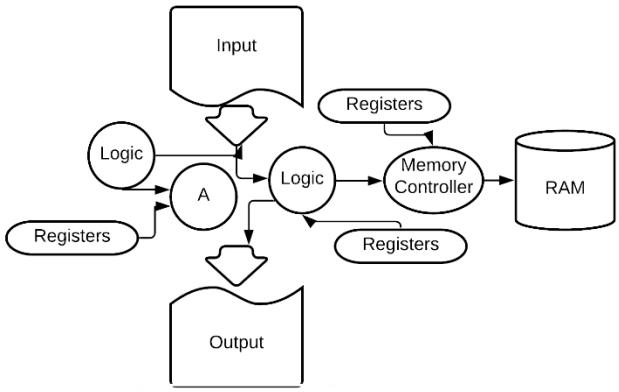

X0Y3
X1Y3
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0


NEXYS A7
DIGILENT
XILINX
ANALOG DEVICES
ARTIX-7
100T
CSG324
QC.OK
9
POWER
USB HOST
ETHERNET
VGA
MONO AUDIO OUT
PROG UART
SD MICRO
BUSY
MODE
CPU RESET
PROG
DONE
MIC
TEMP SENSOR
BTNU (M18)
BTNC (N17)
BTNL (P17)
BTNR (M17)
BTND (P18)

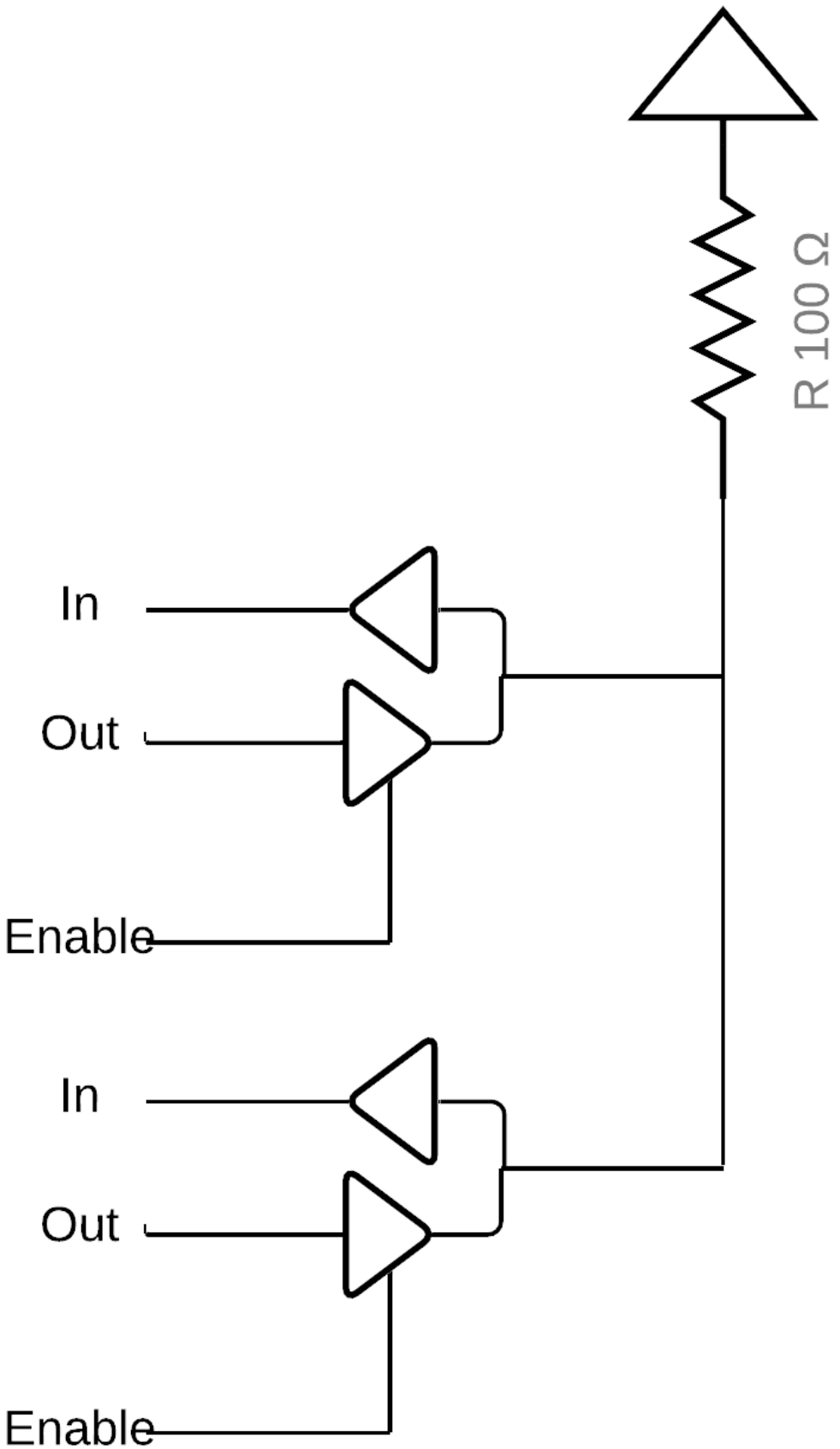
Chapter 2: Combinational Logic

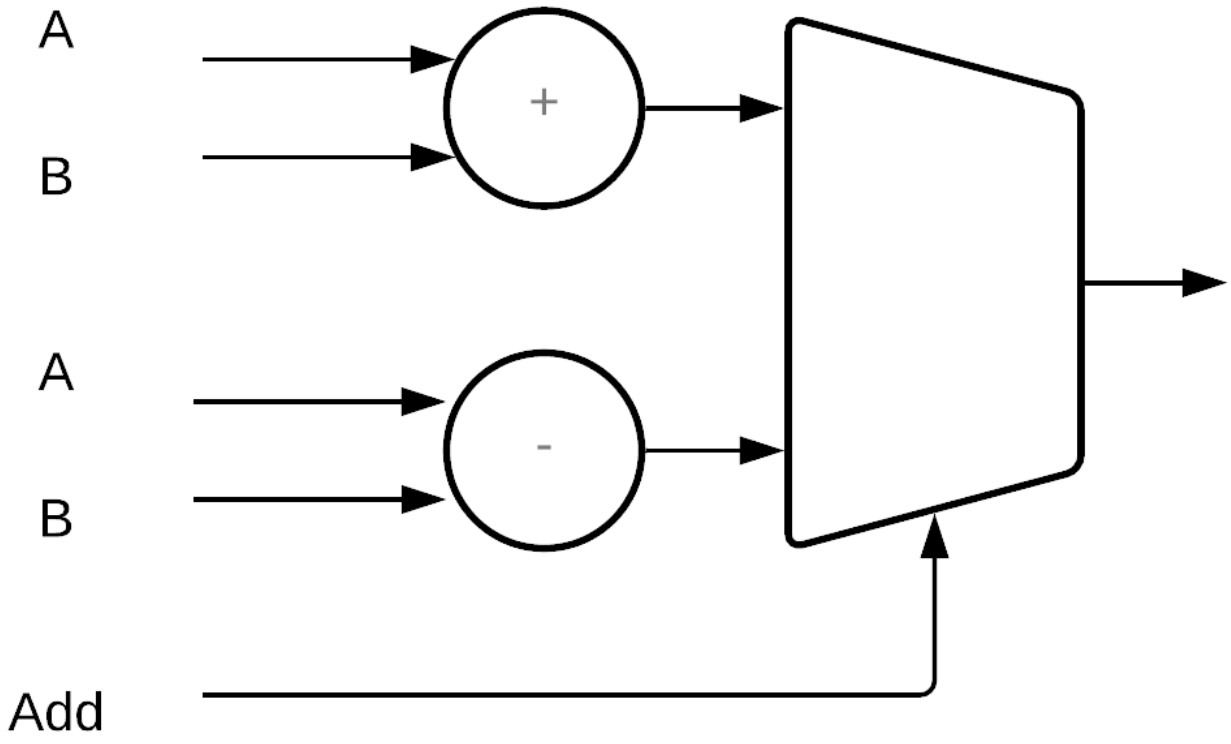


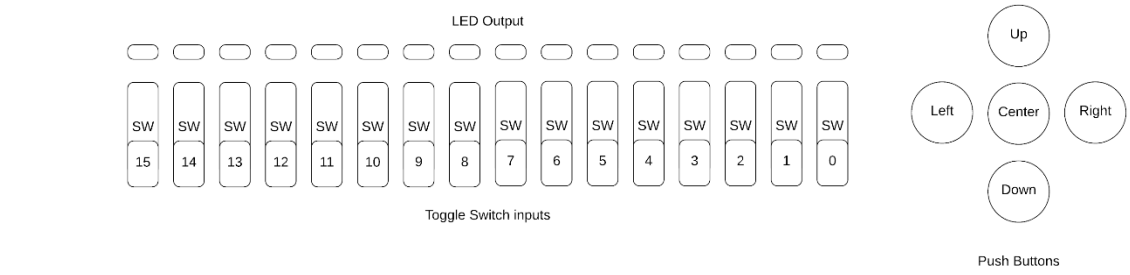
Traditional computing flow

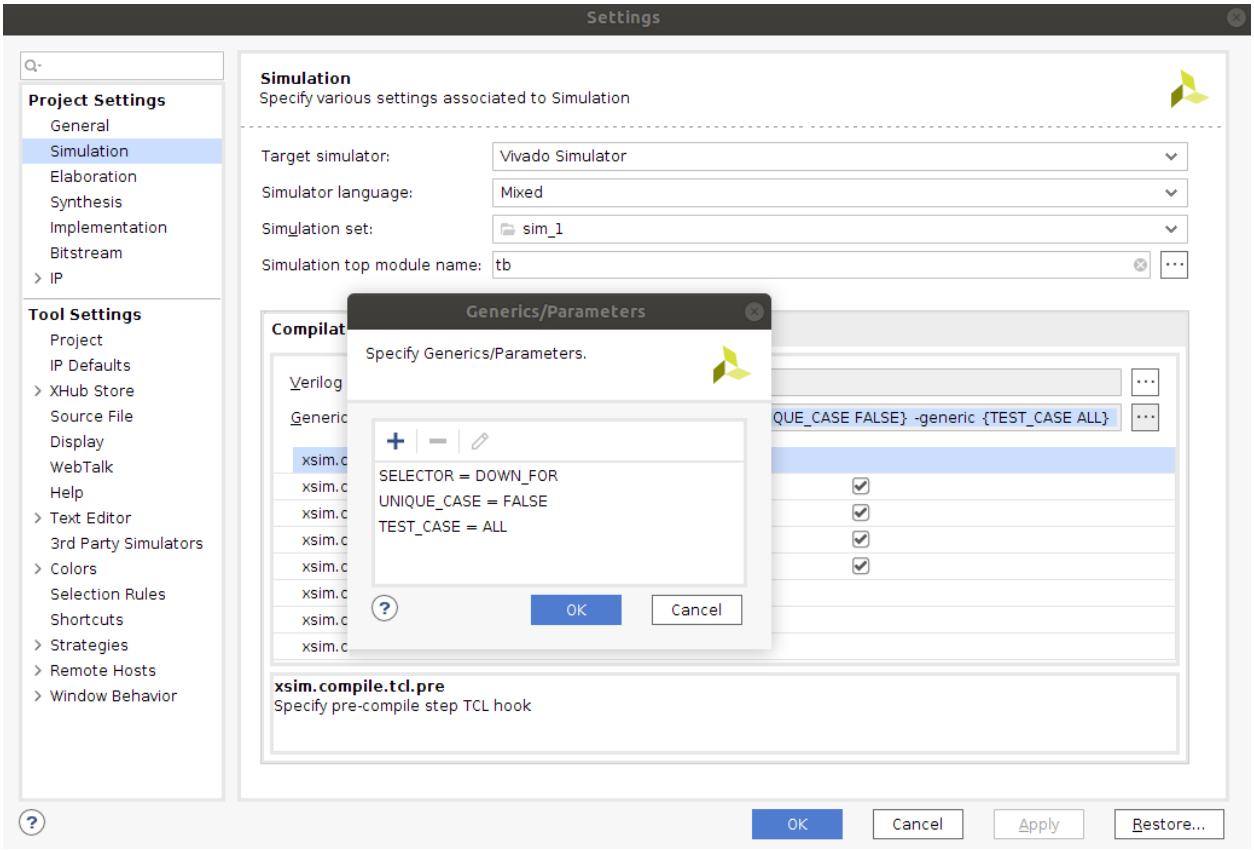


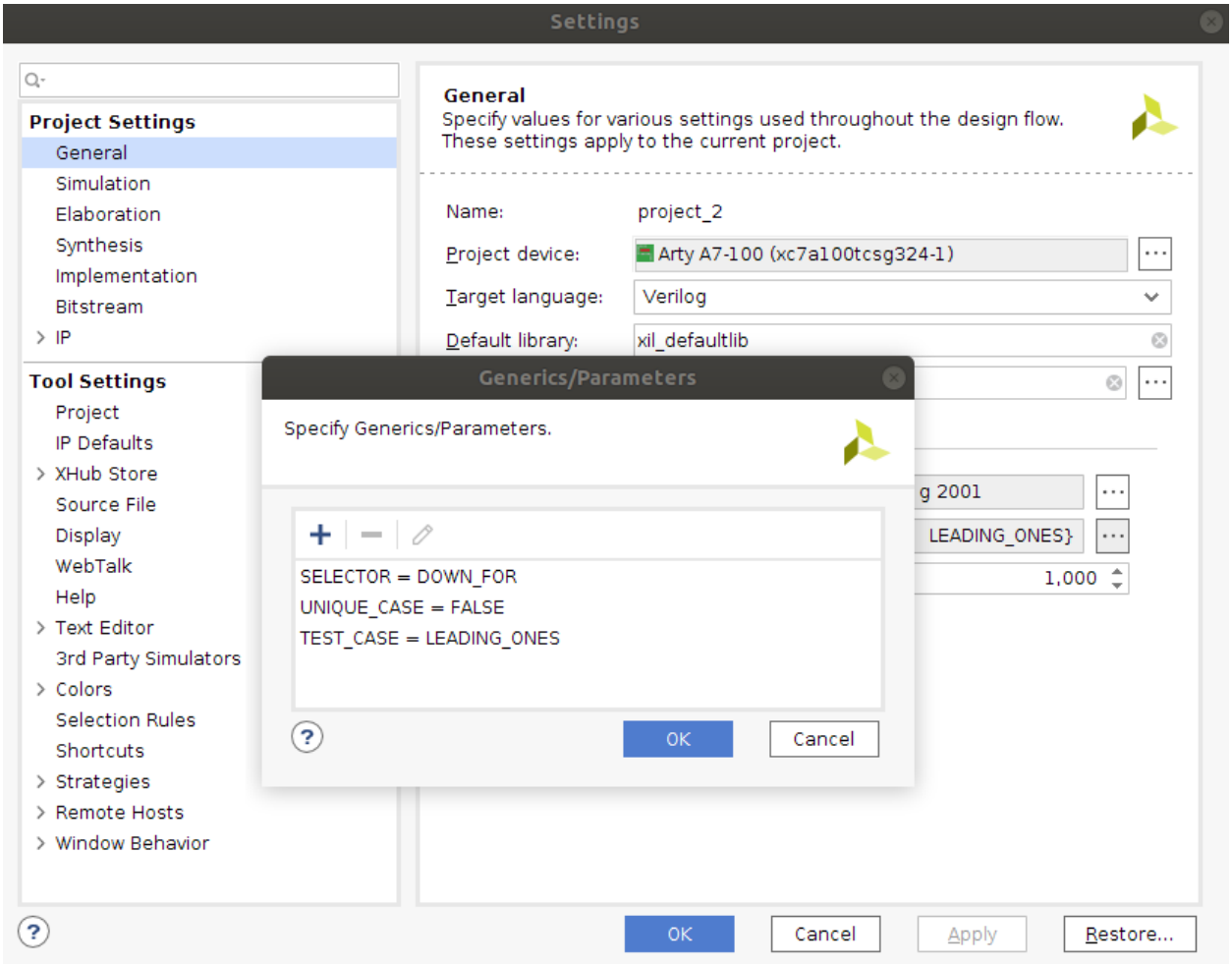
HDL generated flow

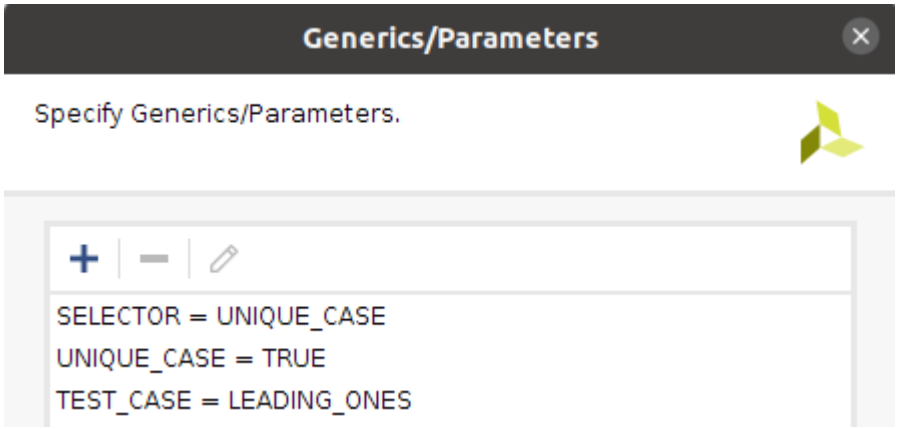

R 100 Ω
In
Out
Enable
In
Out
Enable


A
B
+
A
B
-
Add


LED Output
SW 15
SW 14
SW 13
SW 12
SW 11
SW 10
SW 9
SW 8
SW 7
SW 6
SW 5
SW 4
SW 3
SW 2
SW 1
SW 0
Toggle Switch inputs
Up
Left
Center
Right
Down
Push Buttons


Settings
Project Settings
General
Simulation
Elaboration
Synthesis
Implementation
Bitstream
IP
Tool Settings
Project
IP Defaults
XHub Store
Source File
Display
WebTalk
Help
Text Editor
3rd Party Simulators
Colors
Selection Rules
Shortcuts
Strategies
Remote Hosts
Window Behavior
Simulation
Specify various settings associated to Simulation
Target simulator:
Vivado Simulator
Simulator language:
Mixed
Simulation set:
sim_1
Simulation top module name:
tb
Generics/Parameters
Specify Generics/Parameters.
SELECTOR = DOWN_FOR
UNIQUE_CASE = FALSE
TEST_CASE = ALL
OK
Cancel
xsim.compile.tcl.pre
Specify pre-compile step TCL hook
OK
Cancel
Apply
Restore...

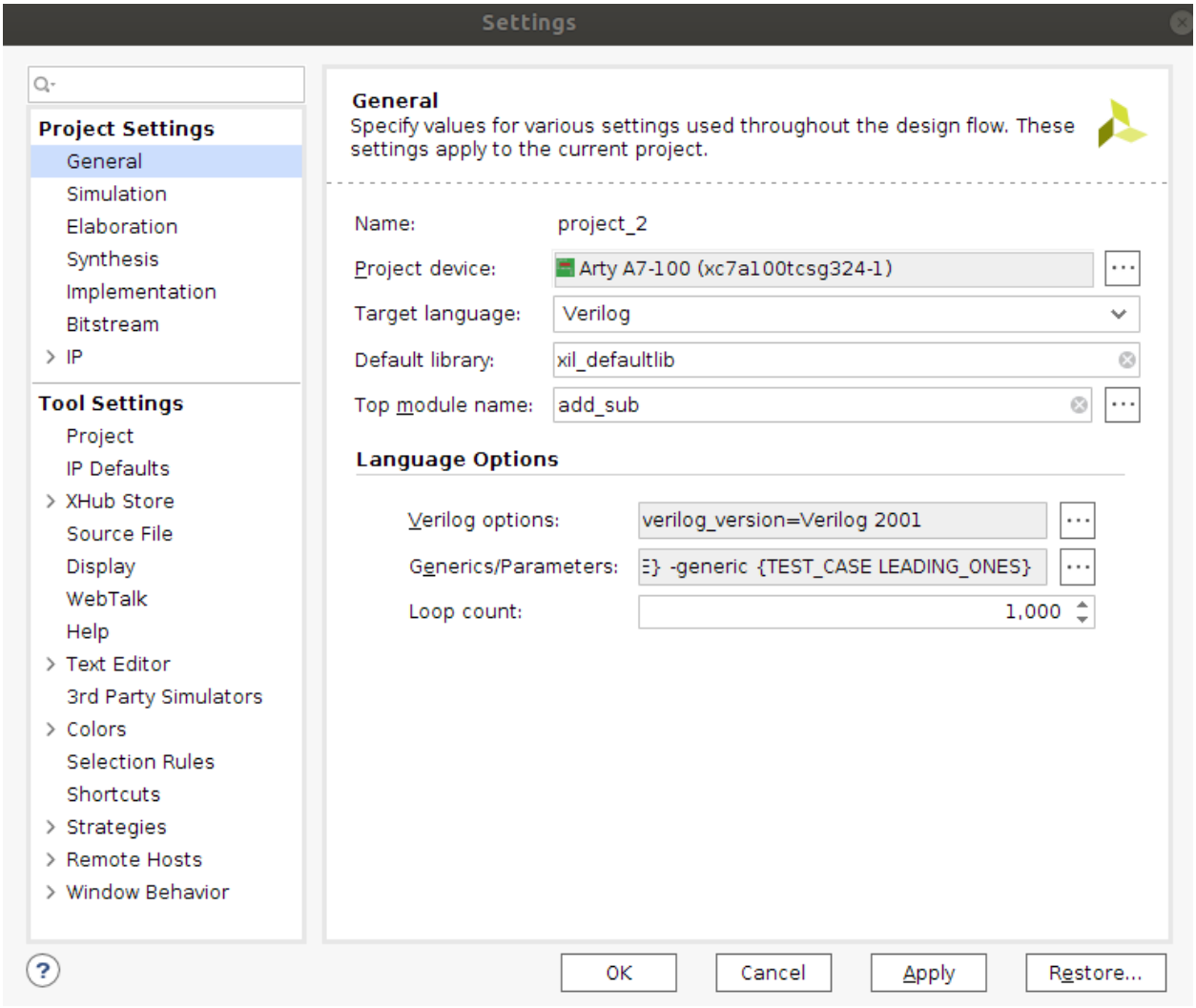

Settings
Project Settings
General
Simulation
Elaboration
Synthesis
Implementation
Bitstream
IP
Tool Settings
Project
IP Defaults
XHub Store
Source File
Display
WebTalk
Help
Text Editor
3rd Party Simulators
Colors
Selection Rules
Shortcuts
Strategies
Remote Hosts
Window Behavior
General
Specify values for various settings used throughout the design flow.
These settings apply to the current project.
Name: project_2
Project device: Arty A7-100 (xc7a100tcsg324-1)
Target language: Verilog
Default library: xil_defaultlib
Generics/Parameters
Specify Generics/Parameters.
SELECTOR = DOWN_FOR
UNIQUE_CASE = FALSE
TEST_CASE = LEADING_ONES
OK
Cancel
g 2001
LEADING_ONES}
1,000
OK
Cancel
Apply
Restore...

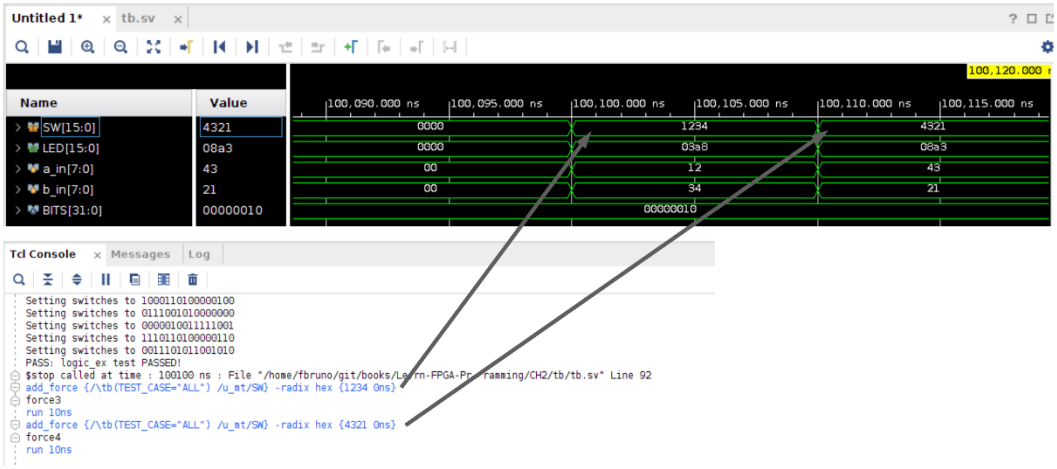

Generics/Parameters
Specify Generics/Parameters.
SELECTOR = UNIQUE_CASE
UNIQUE_CASE = TRUE
TEST_CASE = LEADING_ONES

Utilization Post-Synthesis | **Post-Implementation**

Graph | **Table**

Resource	Utilization	Available	Utilization %
LUT	7	63400	0.01
IO	21	210	10.00





Utilization Post-Synthesis | **Post-Implementation**

Graph | **Table**

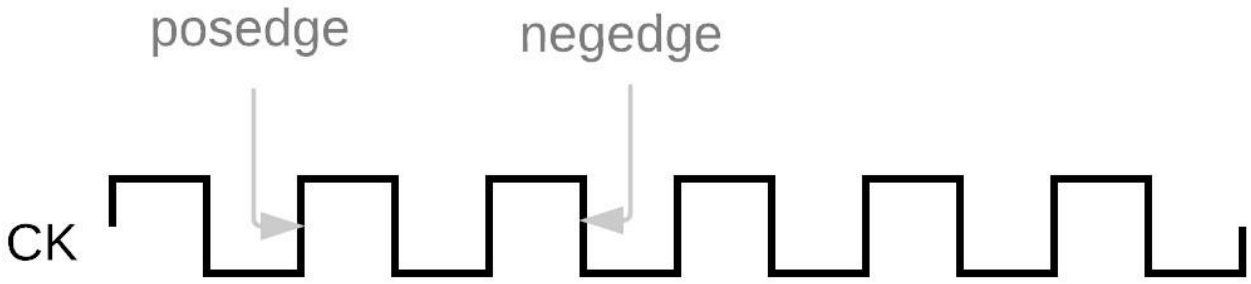
Resource	Utilization	Available	Utilization %
LUT	61	63400	0.10
IO	32	210	15.24

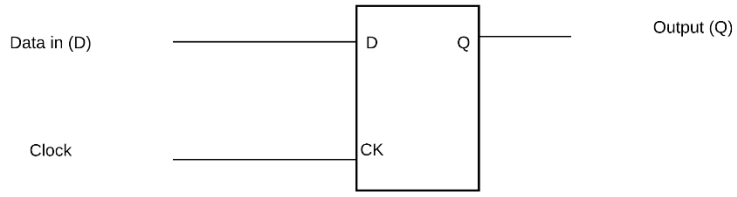
Utilization Post-Synthesis | **Post-Implementation**

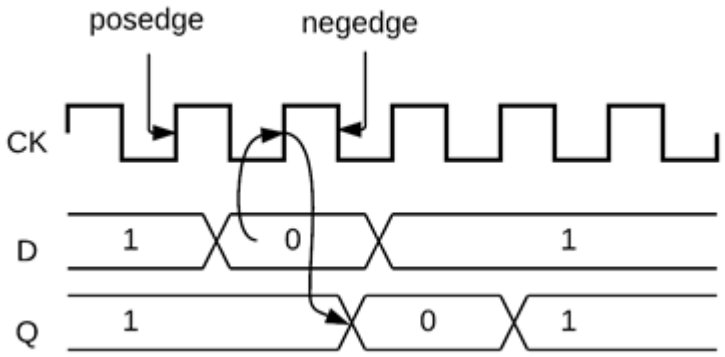
Graph | **Table**

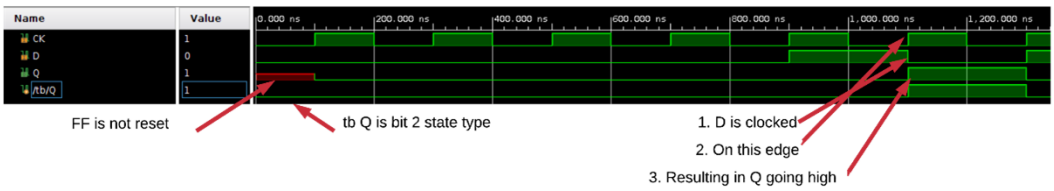
Resource	Utilization	Available	Utilization %
LUT	134	63400	0.21
IO	37	210	17.62

Chapter 3: Counting Button Presses







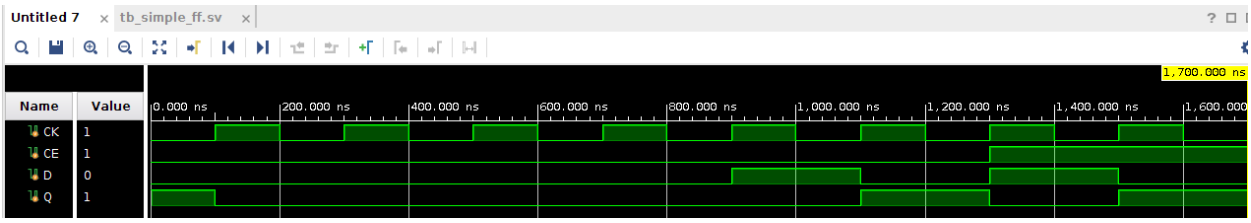


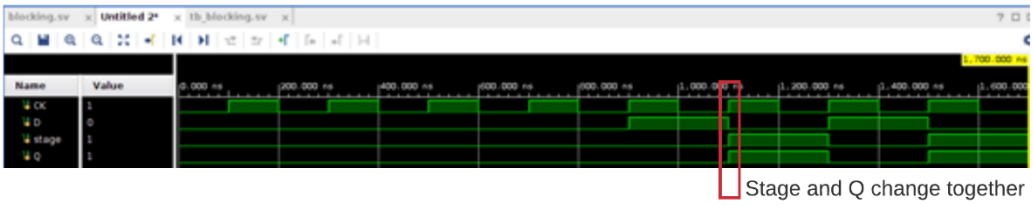
Simulation (2 errors)

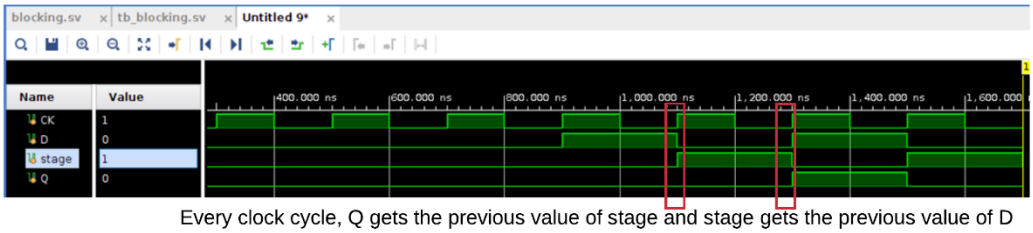
sim_1 (2 errors)

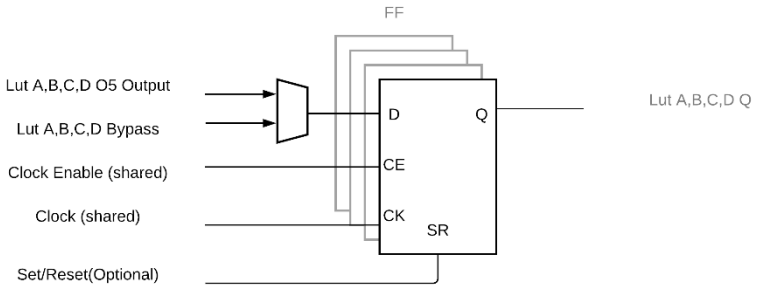
[VRFC 10-3818] variable 'Q' is driven by invalid combination of procedural drivers [simple_init_ff.sv:6]

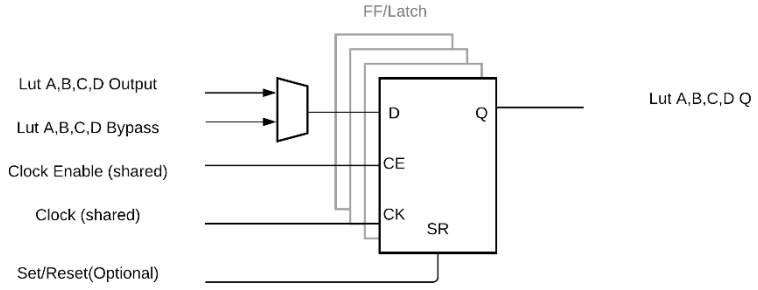
[XSIM 43-3322] Static elaboration of top level Verilog design unit(s) in library work failed.

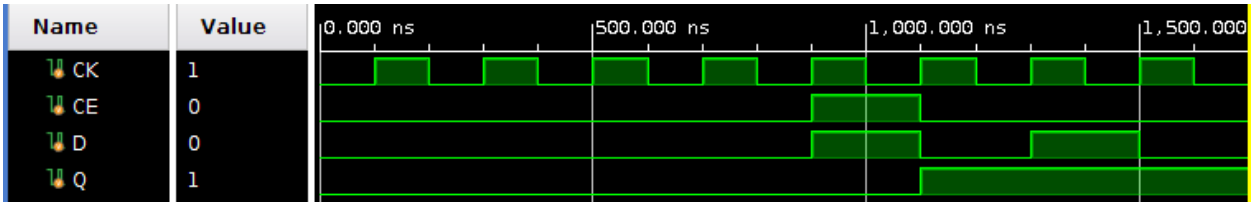

Untitled 7
tb_simple_ff.sv
Name
Value
CK
CE
D
Q
1
1
0
1
0.000 ns
200.000 ns
400.000 ns
600.000 ns
800.000 ns
1,000.000 ns
1,200.000 ns
1,400.000 ns
1,600.000
1,700.000 ns

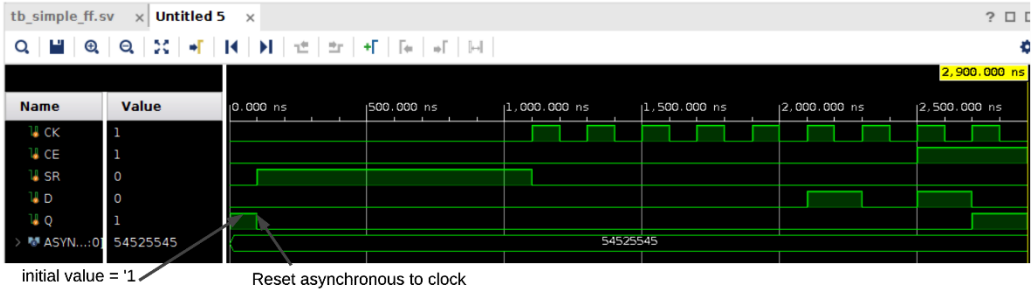

blocking.sv
Untitled 2*
tb_blocking.sv
Name
Value
CK
D
stage
Q
Stage and Q change together

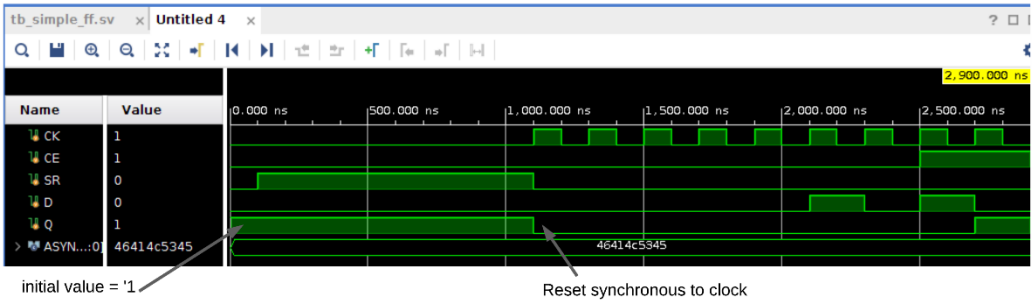

blocking.sv
tb_blocking.sv
Untitled 9*
Name
Value
CK
D
stage
Q
Every clock cycle, Q gets the previous value of stage and stage gets the previous value of D

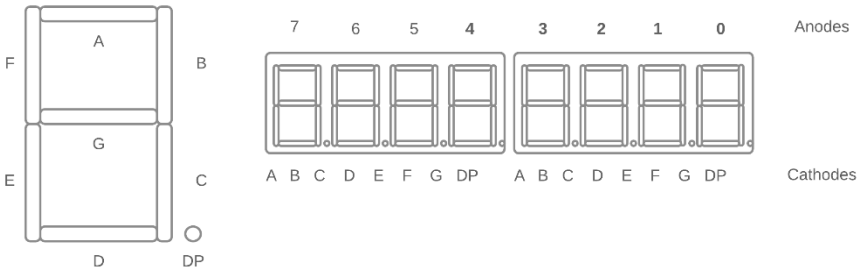

FF
Lut A,B,C,D O5 Output
Lut A,B,C,D Bypass
Clock Enable (shared)
Clock (shared)
Set/Reset(Optional)
D
Q
CE
CK
SR
Lut A,B,C,D Q

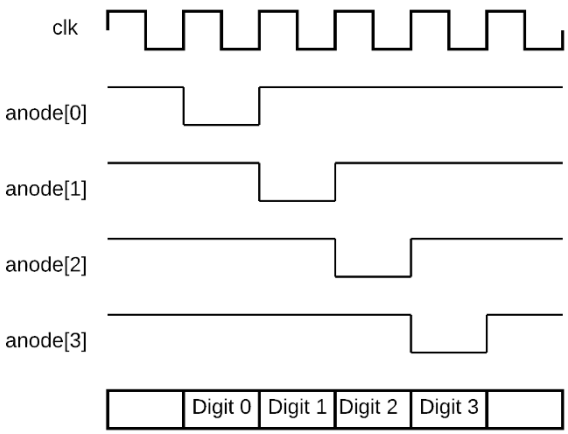

FF/Latch
Lut A,B,C,D Output
Lut A,B,C,D Bypass
Clock Enable (shared)
Clock (shared)
Set/Reset(Optional)
D
Q
CE
CK
SR
Lut A,B,C,D Q

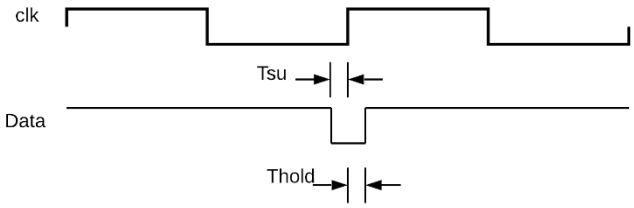

Name
Value
CK
CE
D
Q
1
0
0
1
0.000 ns
500.000 ns
1,000.000 ns
1,500.000

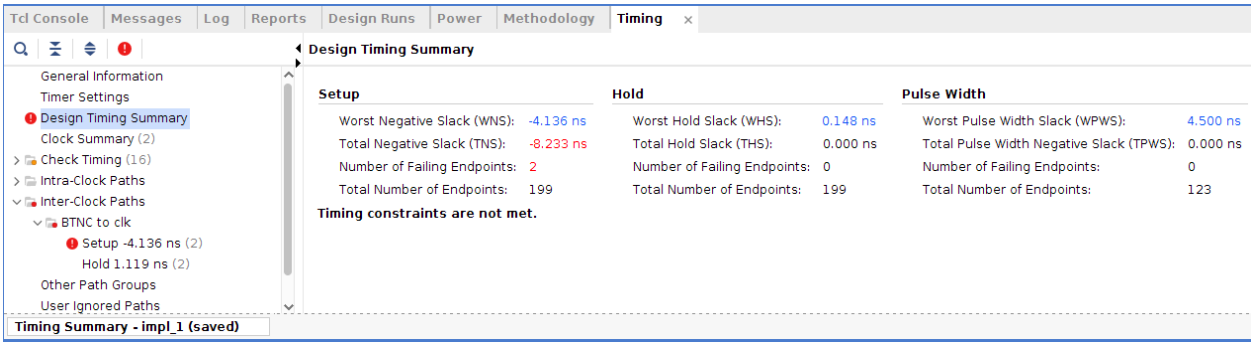

tb_simple_ff.sv
Untitled 5
Name
Value
CK
CE
SR
D
Q
ASYN...:0]
1
1
0
0
1
54525545
2,900.000 ns
0.000 ns
500.000 ns
1,000.000 ns
1,500.000 ns
2,000.000 ns
2,500.000 ns
54525545
initial value = '1
Reset asynchronous to clock

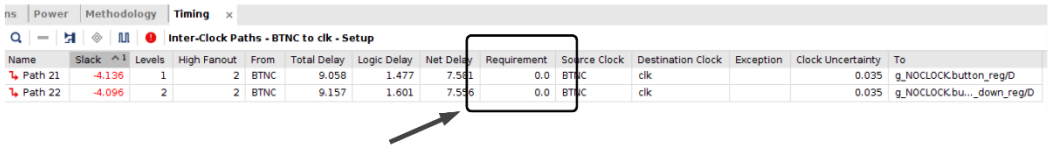

tb_simple_ff.sv
Untitled 4
Name
Value
CK
CE
SR
D
Q
ASYN...:0]
1
1
0
0
1
46414c5345
2,900.000 ns
0.000 ns
500.000 ns
1,000.000 ns
1,500.000 ns
2,000.000 ns
2,500.000 ns
46414c5345
initial value = '1
Reset synchronous to clock

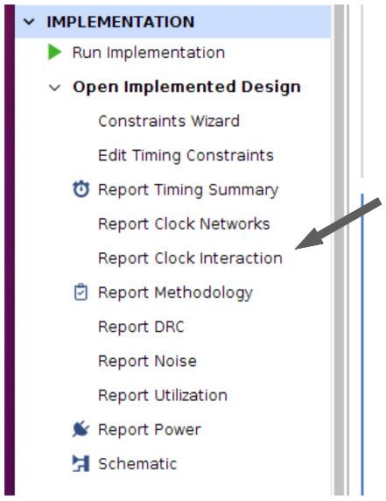

A
B
C
D
E
F
G
DP
7 6 5 4 3 2 1 0
Anodes
A B C D E F G DP A B C D E F G DP
Cathodes

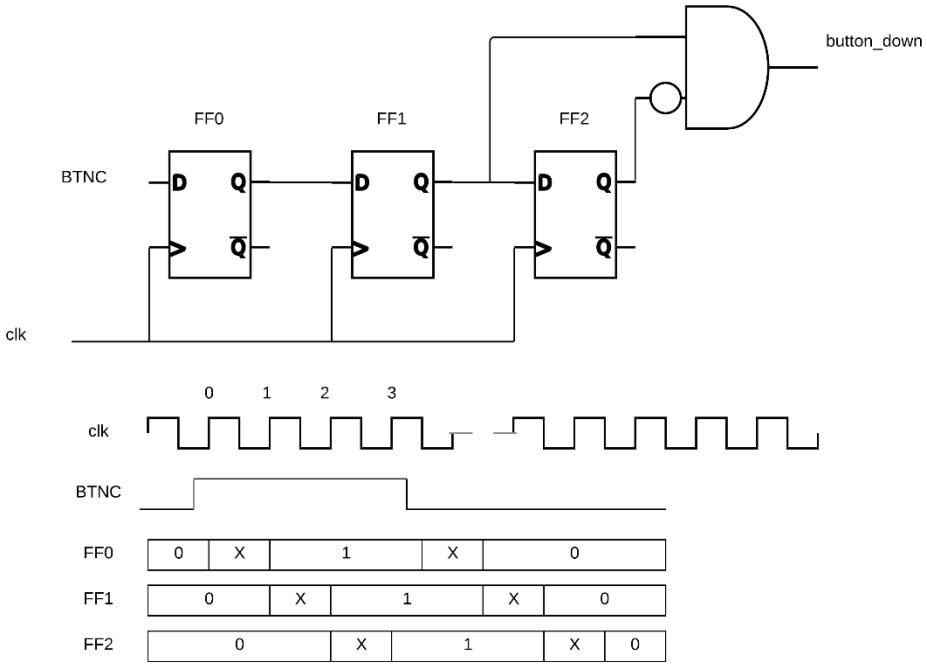

clk
anode[0]
anode[1]
anode[2]
anode[3]
Digit 0
Digit 1
Digit 2
Digit 3


clk
Tsu
Data
Thold


Tcl Console
Messages
Log
Reports
Design Runs
Power
Methodology
Timing
Design Timing Summary
General Information
Timer Settings
Design Timing Summary
Clock Summary (2)
Check Timing (16)
Intra-Clock Paths
Inter-Clock Paths
BTNC to clk
Setup -4.136 ns (2)
Hold 1.119 ns (2)
Other Path Groups
User Ignored Paths
Setup
Worst Negative Slack (WNS): -4.136 ns
Total Negative Slack (TNS): -8.233 ns
Number of Failing Endpoints: 2
Total Number of Endpoints: 199
Hold
Worst Hold Slack (WHS): 0.148 ns
Total Hold Slack (THS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 199
Pulse Width
Worst Pulse Width Slack (WPWS): 4.500 ns
Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 123
Timing constraints are not met.
Timing Summary - impl_1 (saved)


Power
Methodology
Timing
Inter-Clock Paths - BTNC to clk - Setup
Name
Slack
Levels
High Fanout
From
Total Delay
Logic Delay
Net Delay
Requirement
Source Clock
Destination Clock
Exception
Clock Uncertainty
To
Path 21 -4.136 1 2 BTNC 9.058 1.477 7.581 0.0 BTNC clk 0.035 g_NOCLOCK.button_reg/D
Path 22 -4.096 2 2 BTNC 9.157 1.601 7.556 0.0 BTNC clk 0.035 g_NOCLOCK.bu..._down_reg/D

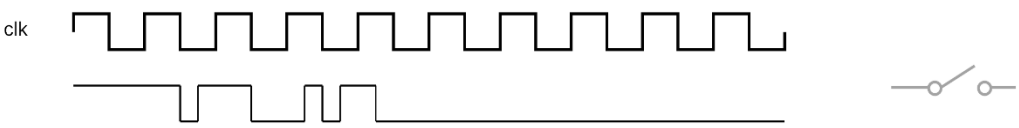


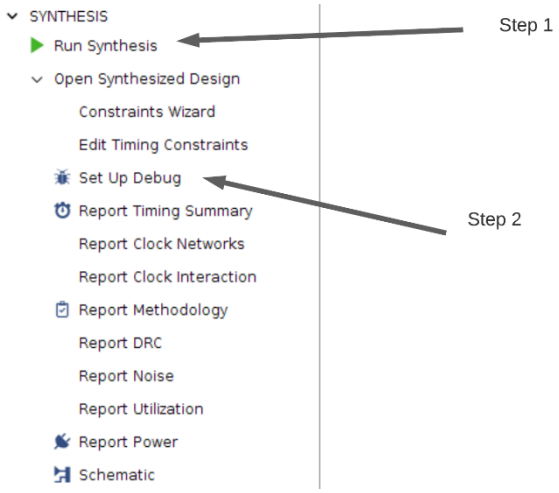


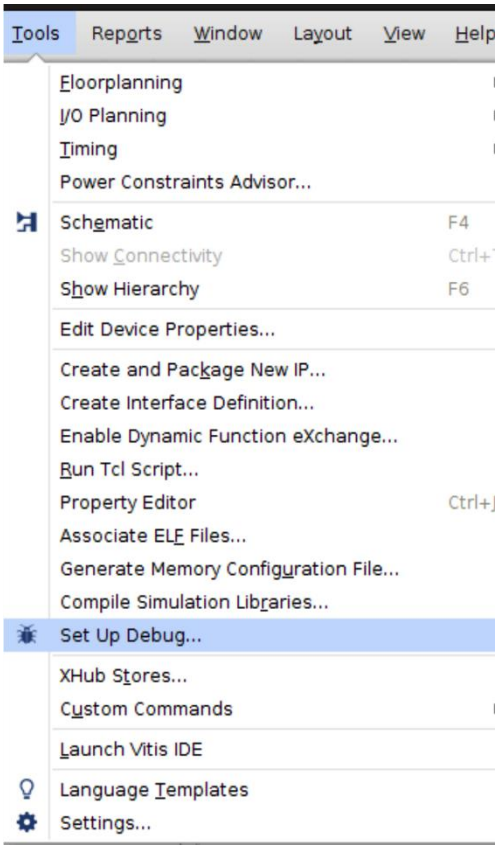
Design Timing Summary

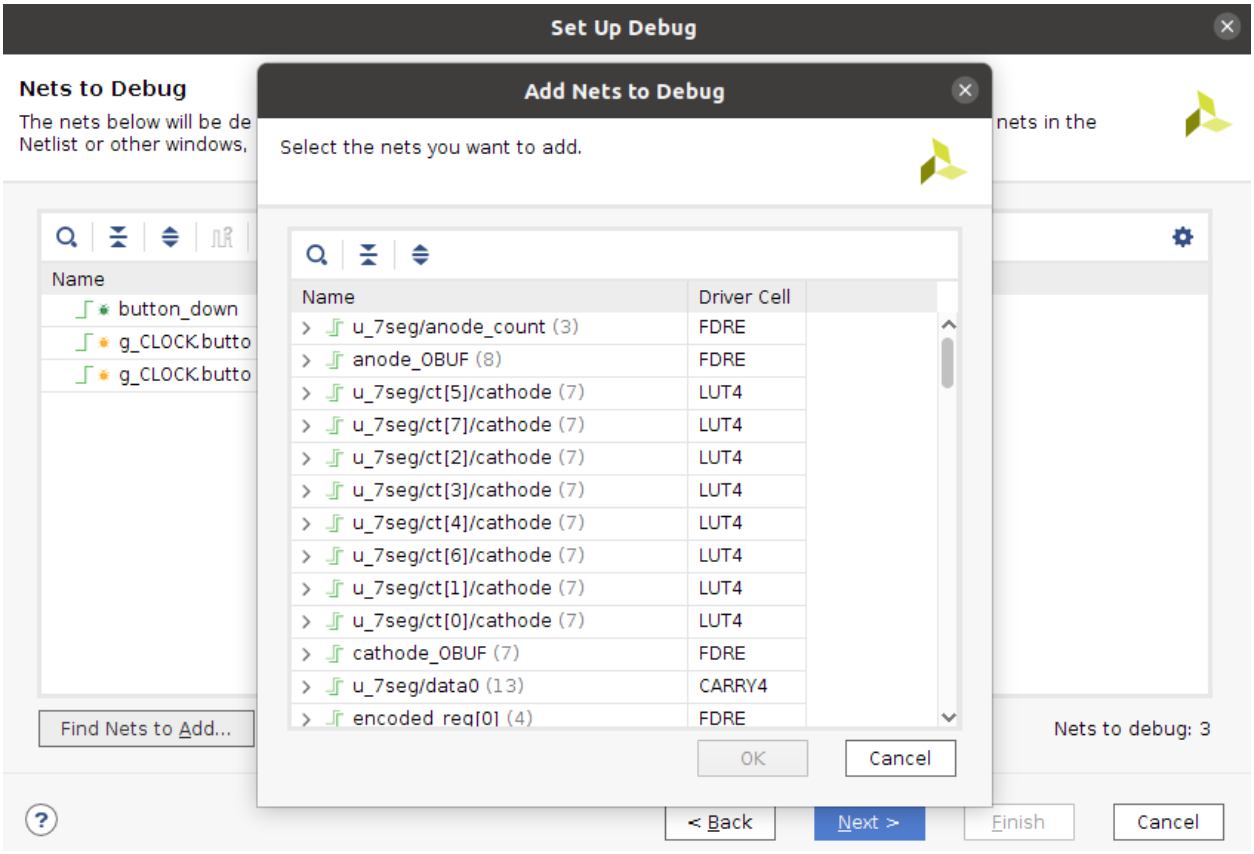
Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	6.498 ns	Worst Hold Slack (WHS):	0.169 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	168	Total Number of Endpoints:	168	Total Number of Endpoints:	125

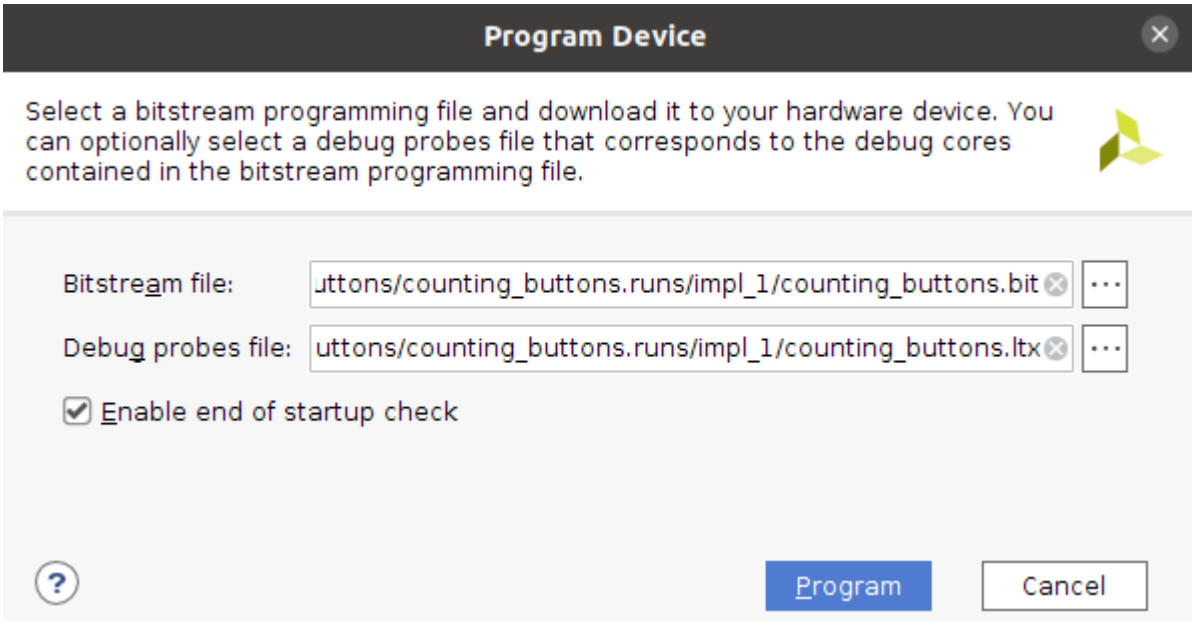
All user specified timing constraints are met.

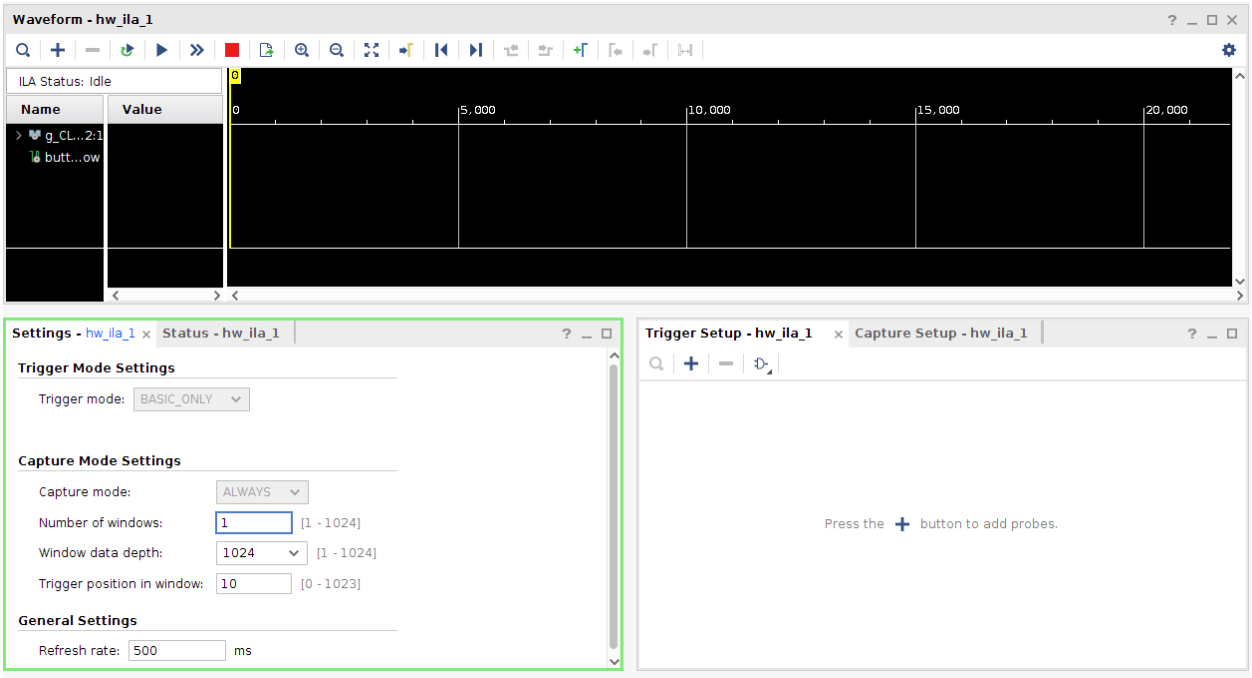

clk

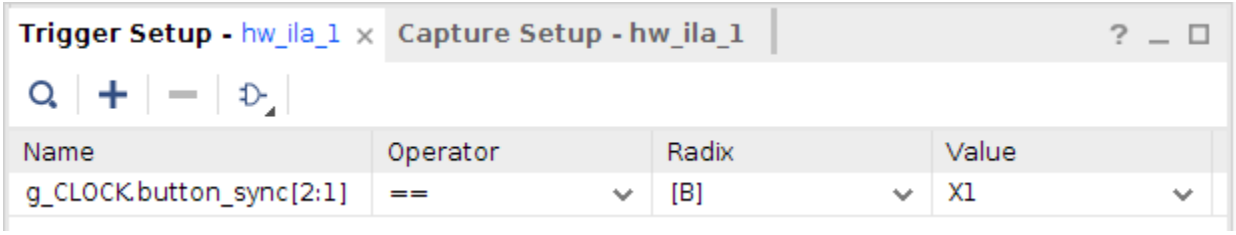

SYNTHESIS
Run Synthesis
Open Synthesized Design
Constraints Wizard
Edit Timing Constraints
Set Up Debug
Report Timing Summary
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Report Noise
Report Utilization
Report Power
Schematic
Step 1
Step 2

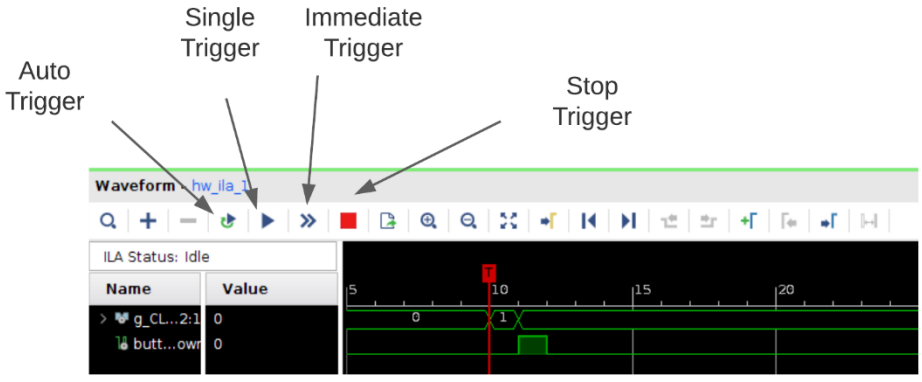

Tools
Reports
Window
Layout
View
Help
Floorplanning
I/O Planning
Timing
Power Constraints Advisor...
Schematic F4
Show Connectivity
Show Hierarchy F6
Edit Device Properties...
Create and Package New IP...
Create Interface Definition...
Enable Dynamic Function eXchange...
Run Tcl Script...
Property Editor
Associate ELF Files...
Generate Memory Configuration File...
Compile Simulation Libraries...
Set Up Debug...
XHub Stores...
Custom Commands
Launch Vitis IDE
Language Templates
Settings...

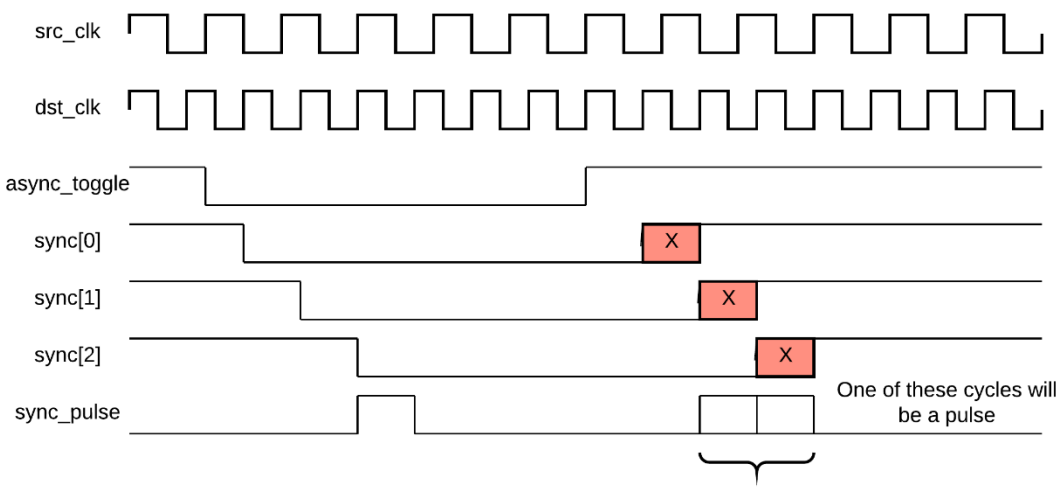

Set Up Debug
Nets to Debug
The nets below will be de
Netlist or other windows,
nets in the
Add Nets to Debug
Select the nets you want to add.
Name
button_down
g_CLOCK.butto
g_CLOCK.butto
Name
Driver Cell
u_7seg/anode_count (3)
FDRE
anode_OBUF (8)
FDRE
u_7seg/ct[5]/cathode (7)
LUT4
u_7seg/ct[7]/cathode (7)
LUT4
u_7seg/ct[2]/cathode (7)
LUT4
u_7seg/ct[3]/cathode (7)
LUT4
u_7seg/ct[4]/cathode (7)
LUT4
u_7seg/ct[6]/cathode (7)
LUT4
u_7seg/ct[1]/cathode (7)
LUT4
u_7seg/ct[0]/cathode (7)
LUT4
cathode_OBUF (7)
FDRE
u_7seg/data0 (13)
CARRY4
encoded_reg[0] (4)
FDRE
OK
Cancel
Find Nets to Add...
Nets to debug: 3
< Back
Next >
Finish
Cancel

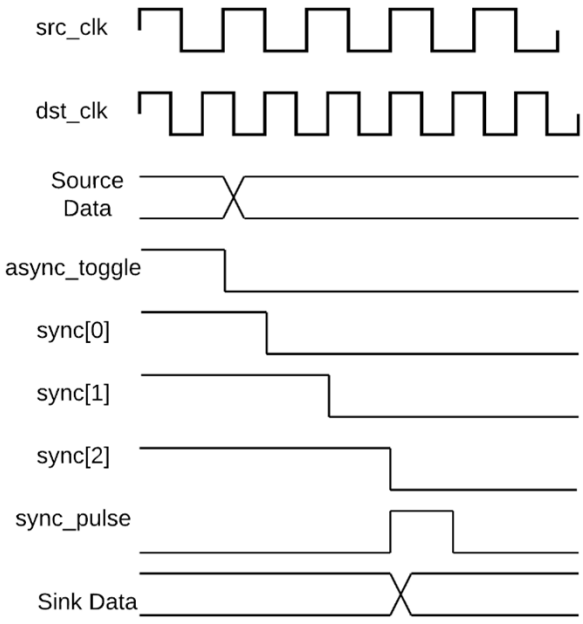

Program Device
Select a bitstream programming file and download it to your hardware device. You can optionally select a debug probes file that corresponds to the debug cores contained in the bitstream programming file.
Bitstream file:
uttons/counting_buttons.runs/impl_1/counting_buttons.bit
Debug probes file:
uttons/counting_buttons.runs/impl_1/counting_buttons.ltx
Enable end of startup check
Program
Cancel


Waveform - hw_ila_1
ILA Status: Idle
Name
Value
g_CL...2:1
butt...ow
0
5,000
10,000
15,000
20,000
Settings - hw_ila_1
Status - hw_ila_1
Trigger Mode Settings
Trigger mode:
BASIC_ONLY
Capture Mode Settings
Capture mode:
ALWAYS
Number of windows:
1
[1 - 1024]
Window data depth:
1024
[1 - 1024]
Trigger position in window:
10
[0 - 1023]
General Settings
Refresh rate:
500
ms
Trigger Setup - hw_ila_1
Capture Setup - hw_ila_1
Press the + button to add probes.

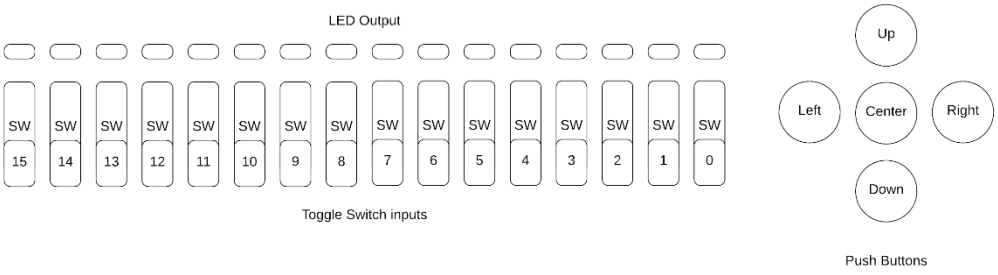

Trigger Setup - hw_ila_1
Capture Setup - hw_ila_1
Name
Operator
Radix
Value
g_CLOCK.button_sync[2:1]
==
[B]
X1

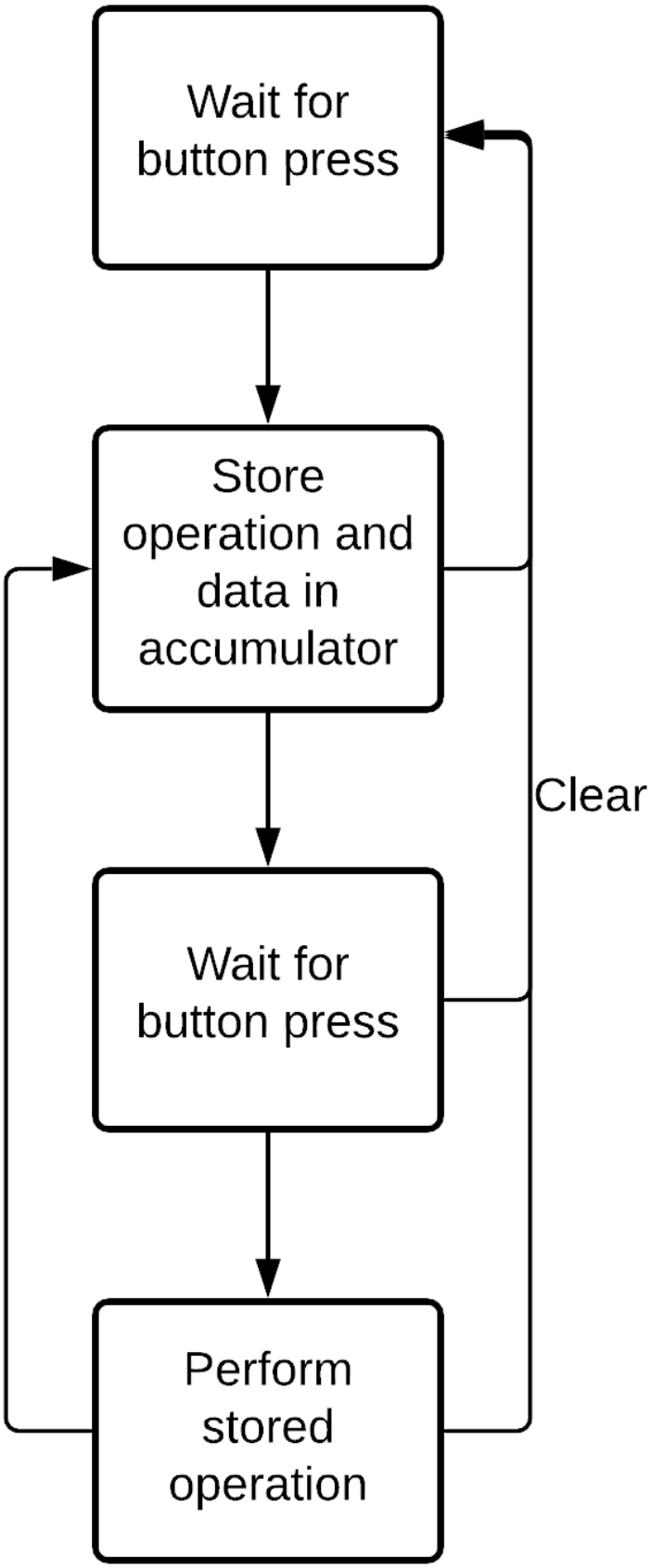

Auto Trigger
Single Trigger
Immediate Trigger
Stop Trigger
Waveform - hw_ila_1
ILA Status: Idle
Name
Value
g_CL...2:1
butt...own
0
0
5
10
15
20
0
1


src_clk
dst_clk
async_toggle
sync[0]
sync[1]
sync[2]
sync_pulse
X
X
X
One of these cycles will be a pulse


src_clk
dst_clk
Source Data
async_toggle
sync[0]
sync[1]
sync[2]
sync_pulse
Sink Data

Chapter 4: Let's Build a Calculator




Wait for button press
Store operation and data in accumulator
Wait for button press
Perform stored operation
Clear

DRC Violations

Summary: 9 warnings

Implemented DRC Report

Timing — **Setup** | Hold | Pulse Width

Worst Negative Slack (WNS):	-4.648 ns
Total Negative Slack (TNS):	-114.321 ns
Number of Failing Endpoints:	37
Total Number of Endpoints:	219

Implemented Timing Report

Utilization — Post-Synthesis | **Post-Implementation**

Graph | **Table**

Resource	Utilization	Available	Utilization %
LUT	535	63400	0.84
FF	191	126800	0.15
DSP	2	240	0.83
IO	38	210	18.10
BUFG	1	32	3.13

Power — **Summary** | On-Chip

Total On-Chip Power:	**0.17 W**
Junction Temperature:	**25.8 °C**
Thermal Margin:	59.2 °C (12.9 W)
Effective θJA:	4.6 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

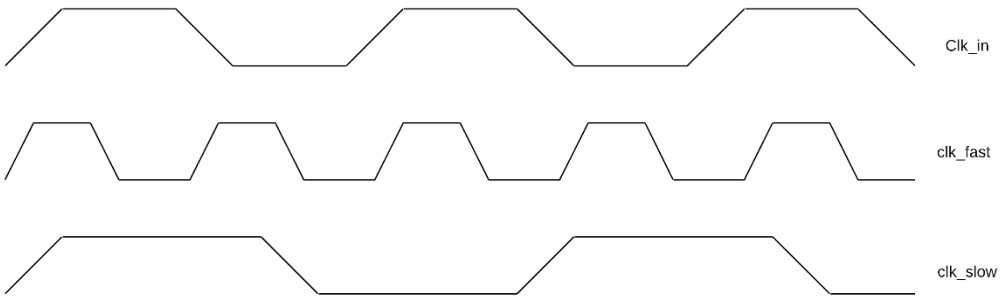
Implemented Power Report

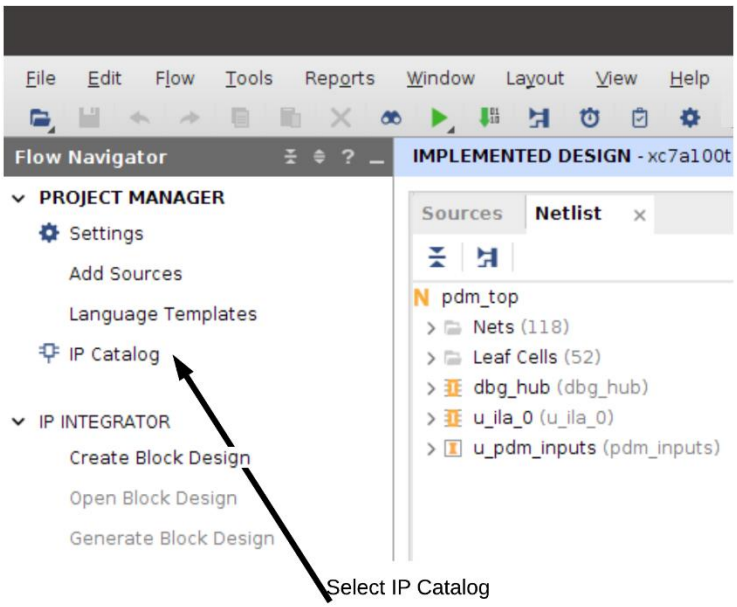
Tcl Console | Messages | Log | Reports | Design Runs | Power | DRC | Methodology | **Timing**

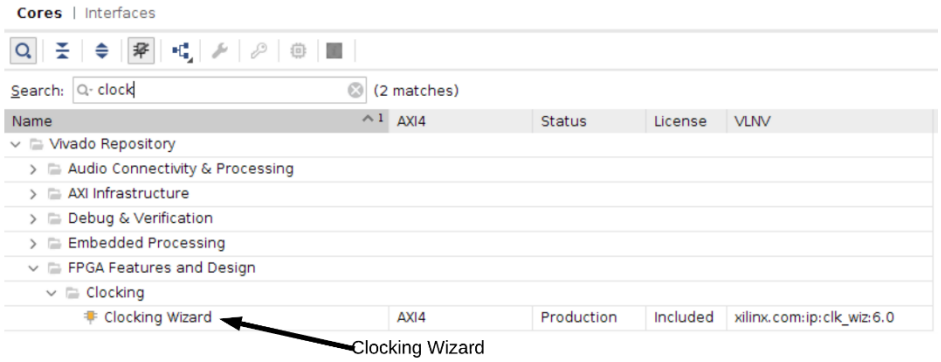
- General Information
- Timer Settings
- Design Timing Summary
- Clock Summary (1)
- Check Timing (36)
- Intra-Clock Paths
  - sys_clk_pin
    - Setup -4.648 ns (10)
    - Hold 0.151 ns (10)
    - Pulse Width 4.500 ns (30)
- Inter-Clock Paths
- Other Path Groups
- User Ignored Paths

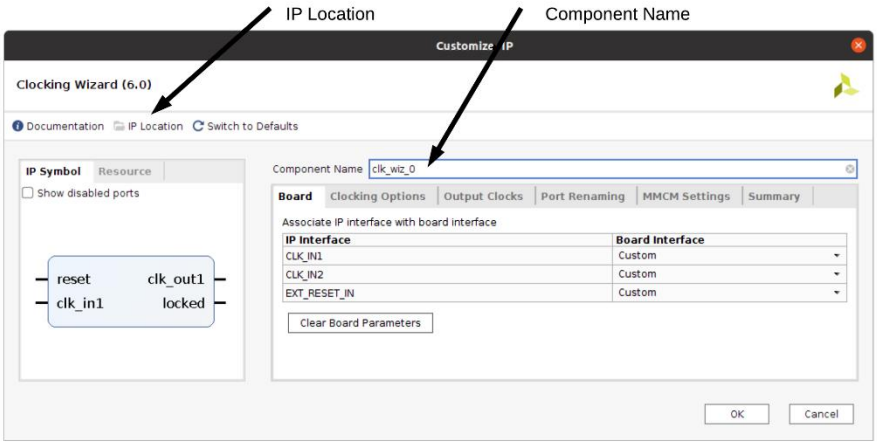
Intra-Clock Paths - sys_clk_pin - Setup

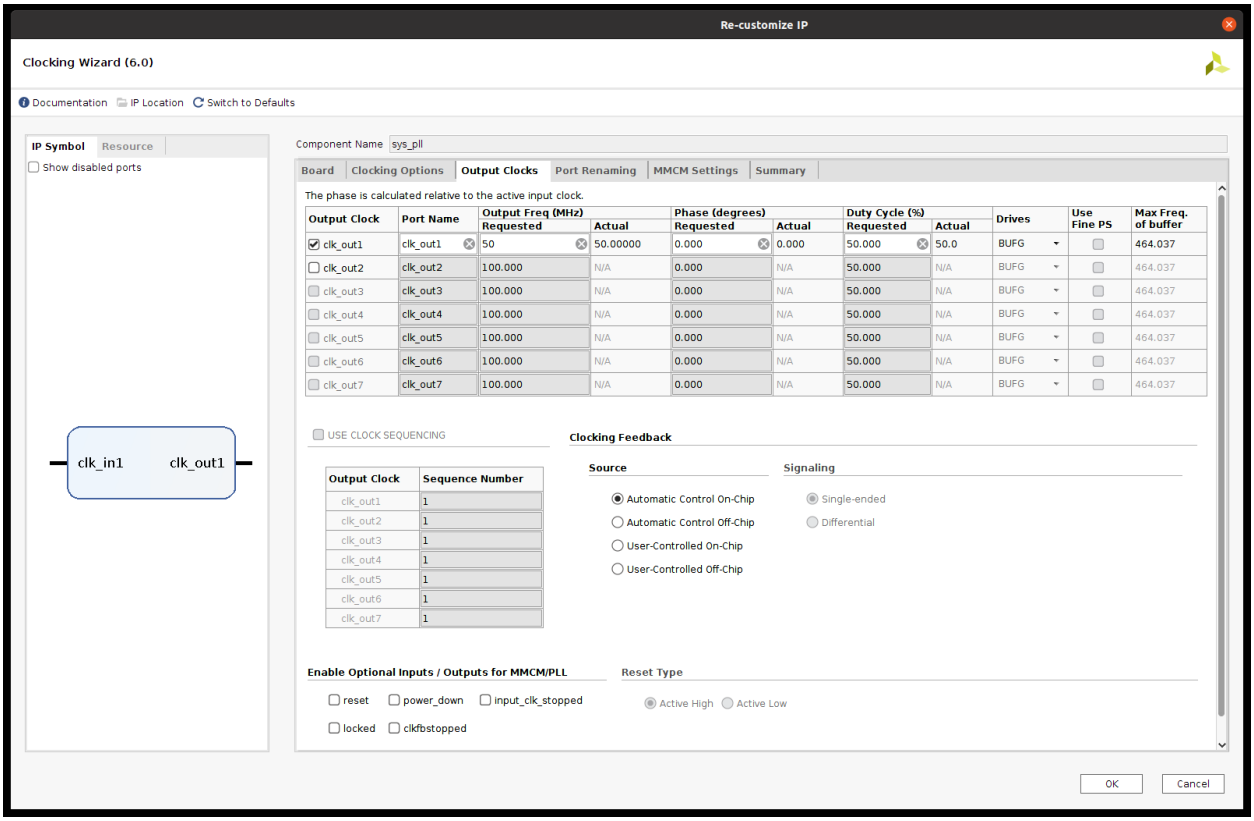
Name	Slack	Levels	High Fanout	From	To	Total Delay
Path 1	-4.648	14	14	g_MEALY.u_sm...or_reg[31]/C	encoded_reg[7][3]/D	14.602
Path 2	-4.644	14	14	g_MEALY.u_sm...or_reg[31]/C	encoded_reg[6][1]/D	14.649
Path 3	-4.635	14	14	g_MEALY.u_sm...or_reg[31]/C	encoded_reg[6][3]/D	14.677
Path 4	-4.560	14	14	g_MEALY.u_sm...or_reg[31]/C	encoded_reg[7][2]/D	14.515
Path 5	-4.554	14	14	g_MEALY.u_sm...or_reg[31]/C	encoded_reg[6][2]/D	14.508
Path 6	-4.541	14	14	g_MEALY.u_sm...or_reg[31]/C	encoded_reg[7][1]/D	14.492
Path 7	-4.538	14	14	g_MEALY.u_sm...or_reg[31]/C	encoded_reg[7][0]/D	14.536
Path 8	-4.240	14	14	g_MEALY.u_sm...or_reg[31]/C	encoded_reg[5][1]/D	14.192
Path 9	-4.229	14	14	g_MEALY.u_sm...or_reg[31]/C	encoded_reg[5][2]/D	14.233
Path 10	-4.220	14	14	g_MEALY.u_sm...or_reg[31]/C	encoded_reg[5][3]/D	14.218




File Edit Flow Tools Reports Window Layout View Help
Flow Navigator
IMPLEMENTED DESIGN - xc7a100t
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
Sources
Netlist
pdm_top
Nets (118)
Leaf Cells (52)
dbg_hub (dbg_hub)
u_ila_0 (u_ila_0)
u_pdm_inputs (pdm_inputs)
Select IP Catalog


Cores | Interfaces
Search: clock (2 matches)
Name
AXI4
Status
License
VLNV
Vivado Repository
Audio Connectivity & Processing
AXI Infrastructure
Debug & Verification
Embedded Processing
FPGA Features and Design
Clocking
Clocking Wizard
AXI4
Production
Included
xilinx.com:ip:clk_wiz:6.0
Clocking Wizard


IP Location
Component Name
Customize IP
Clocking Wizard (6.0)
Documentation
IP Location
Switch to Defaults
IP Symbol
Resource
Show disabled ports
reset
clk_in1
clk_out1
locked
Component Name
clk_wiz_0
Board
Clocking Options
Output Clocks
Port Renaming
MMCM Settings
Summary
Associate IP interface with board interface
IP Interface
Board Interface
CLK_IN1
CLK_IN2
EXT_RESET_IN
Custom
Clear Board Parameters
OK
Cancel



DRC Violations

Summary: 9 warnings

Implemented DRC Report

Timing

Setup | Hold | Pulse Width

Worst Negative Slack (WNS):	2.541 ns
Total Negative Slack (TNS):	0 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	219

Implemented Timing Report

Utilization

Post-Synthesis | **Post-Implementation**

Graph | **Table**

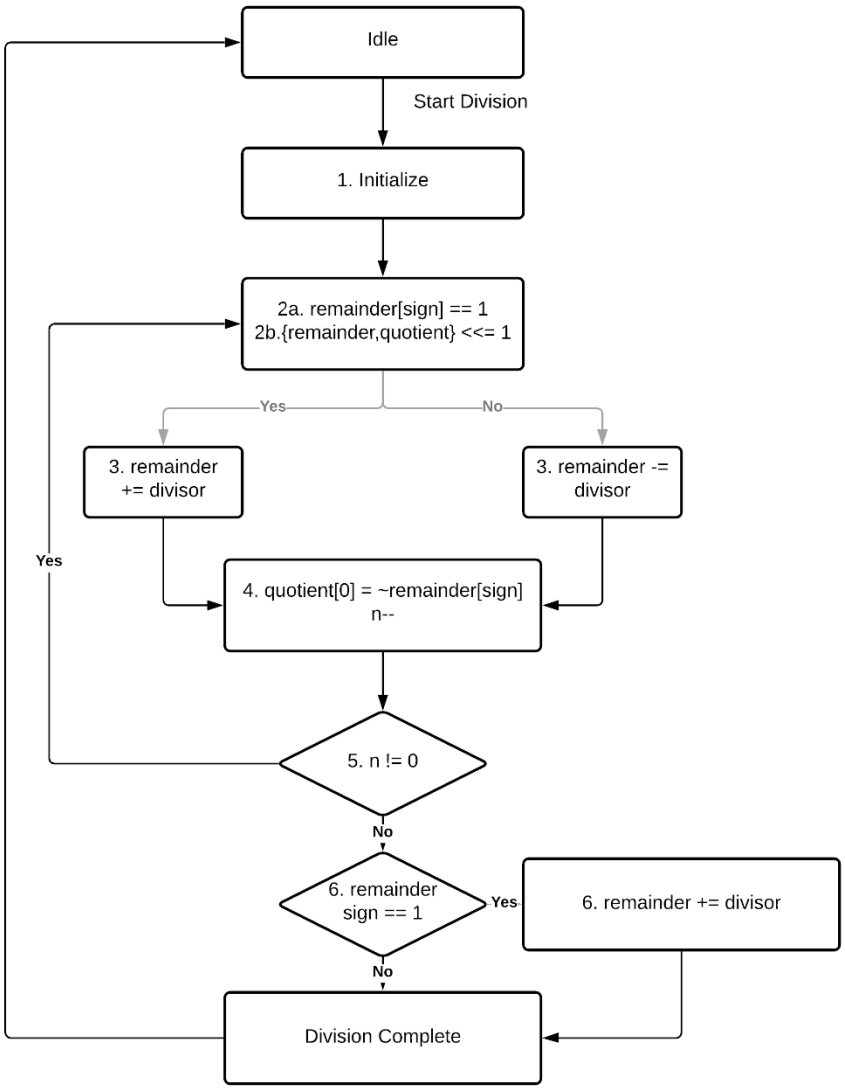
Resource	Utilization	Available	Utilization %
LUT	489	63400	0.77
FF	191	126800	0.15
DSP	2	240	0.83
IO	38	210	18.10
BUFG	2	32	6.25
MMCM	1	6	16.67

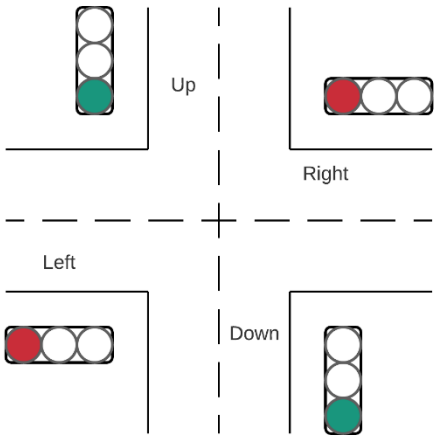
Power

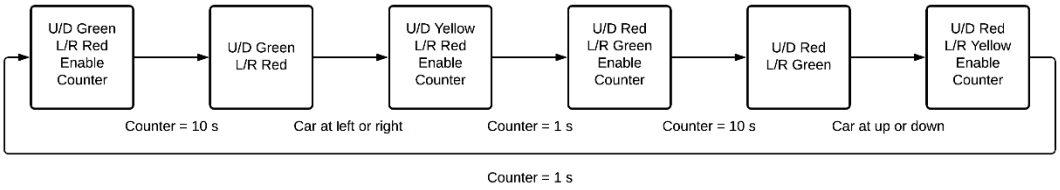
Summary | On-Chip

Total On-Chip Power:	**0.239 W**
Junction Temperature:	**26.1 °C**
Thermal Margin:	58.9 °C (12.8 W)
Effective θJA:	4.6 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

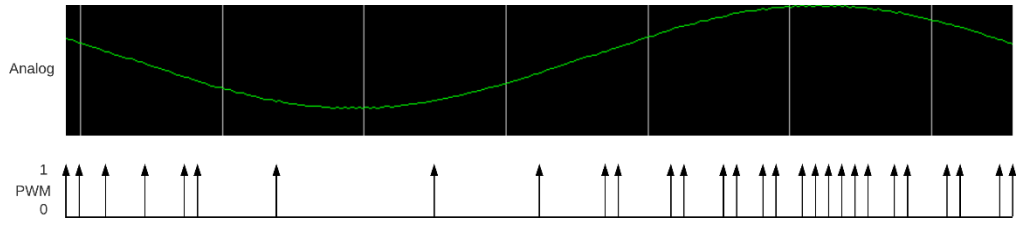
Implemented Power Report

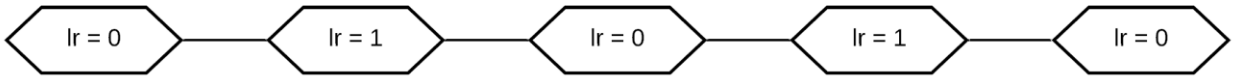

Idle
Start Division
1. Initialize
2a. remainder[sign] == 1
2b.{remainder,quotient} <<= 1
Yes
No
3. remainder
+= divisor
3. remainder -=
divisor
Yes
4. quotient[0] = ~remainder[sign]
n--
5. n != 0
No
6. remainder
sign == 1
Yes
6. remainder += divisor
No
Division Complete

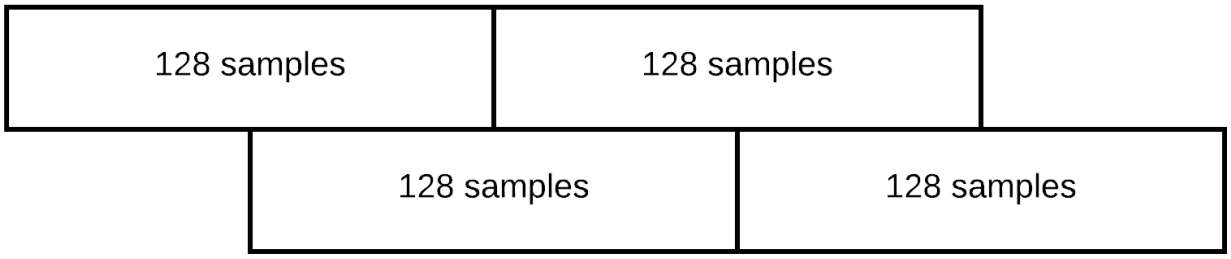

Up
Right
Left
Down

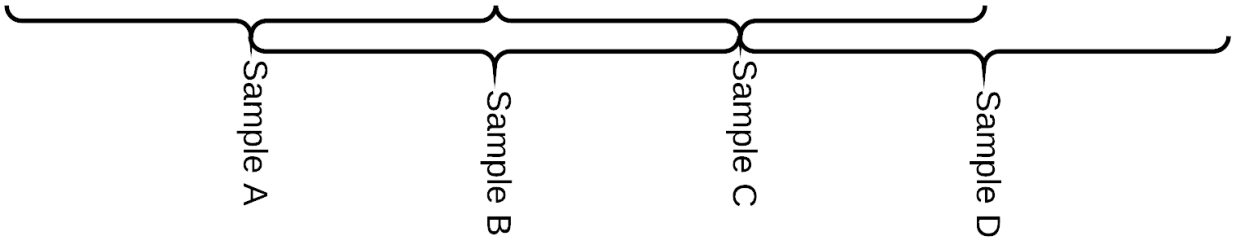

U/D Green
L/R Red
Enable
Counter
U/D Green
L/R Red
U/D Yellow
L/R Red
Enable
Counter
U/D Red
L/R Green
Enable
Counter
U/D Red
L/R Green
U/D Red
L/R Yellow
Enable
Counter
Counter = 10 s
Car at left or right
Counter = 1 s
Counter = 10 s
Car at up or down
Counter = 1 s

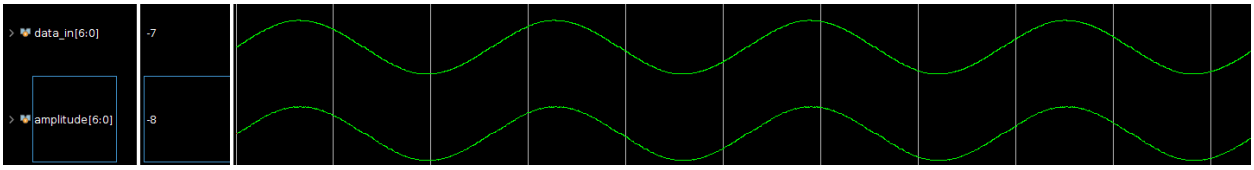
Chapter 5: FPGA Resources and How to Use Them

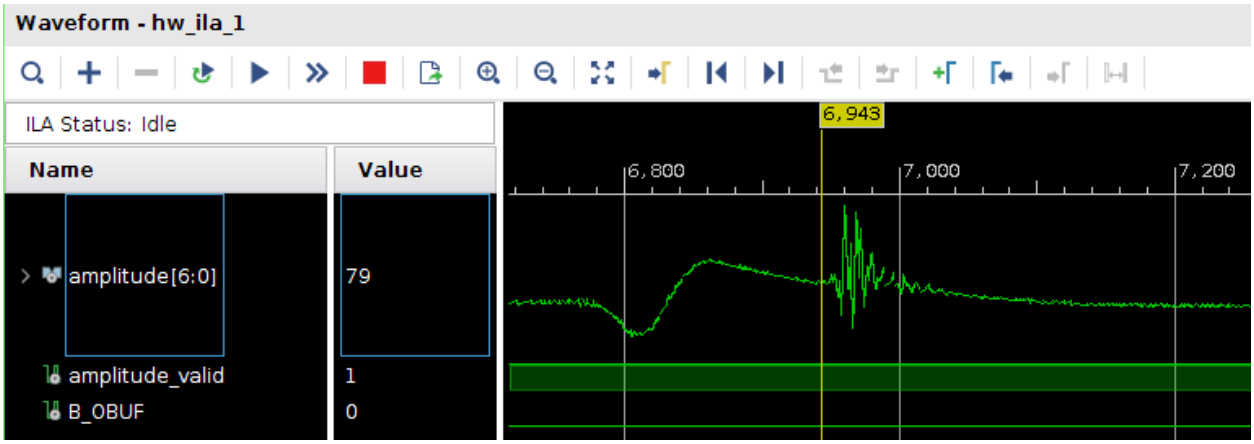


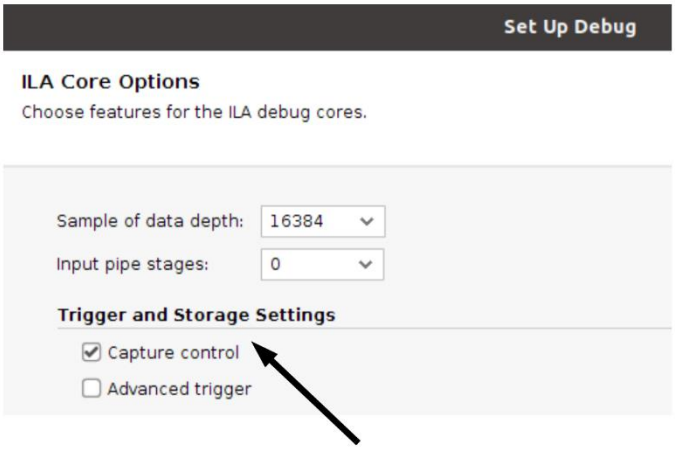


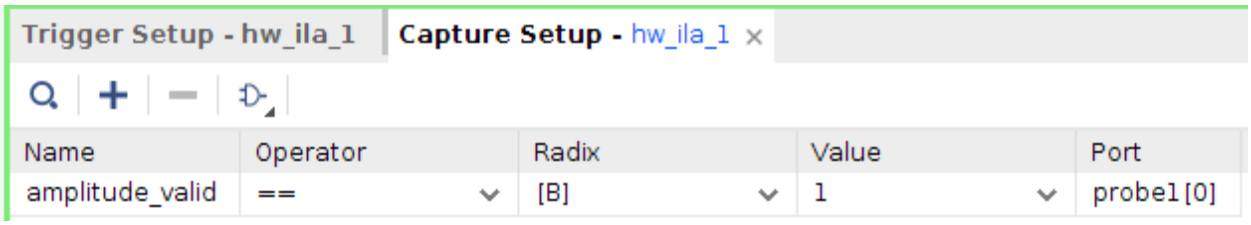


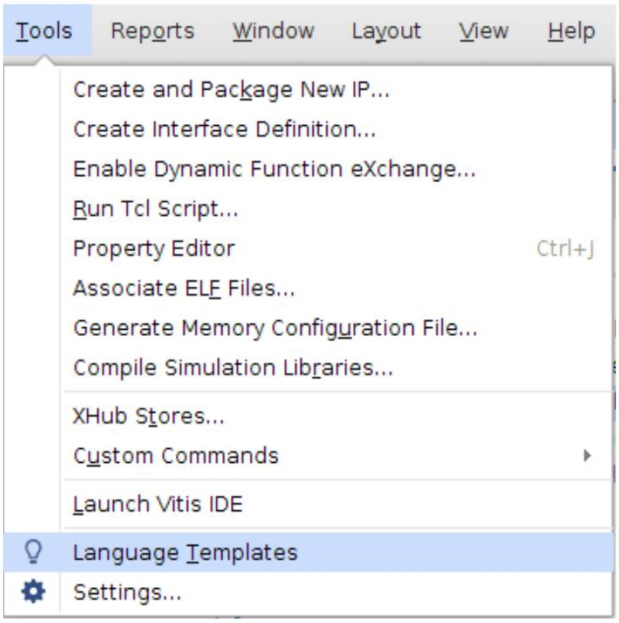


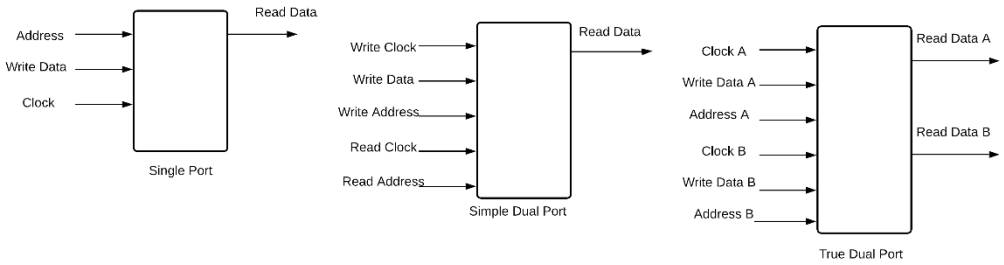


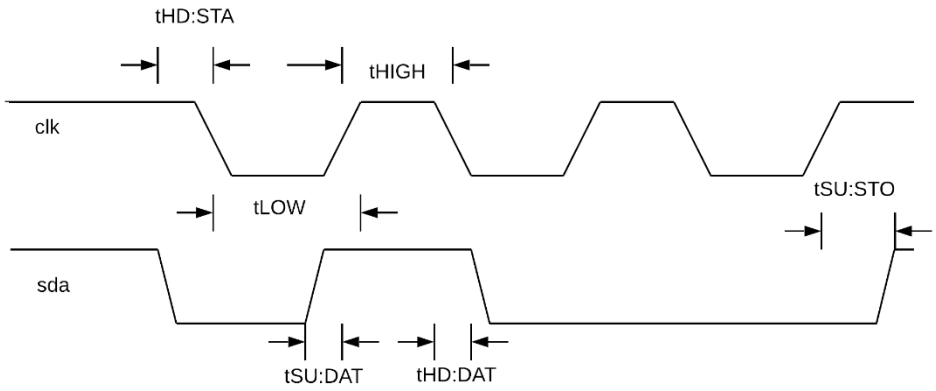

Waveform - hw_ila_1
ILA Status: Idle
Name
Value
amplitude[6:0]
79
amplitude_valid
1
B_OBUF
0
6,943
6,800
7,000
7,200

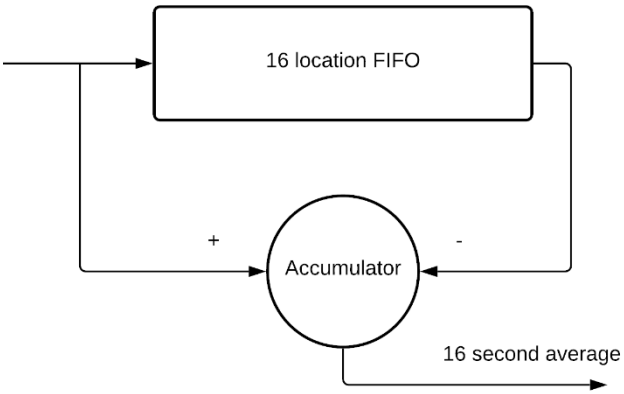

Set Up Debug
ILA Core Options
Choose features for the ILA debug cores.
Sample of data depth:
16384
Input pipe stages:
0
Trigger and Storage Settings
Capture control
Advanced trigger

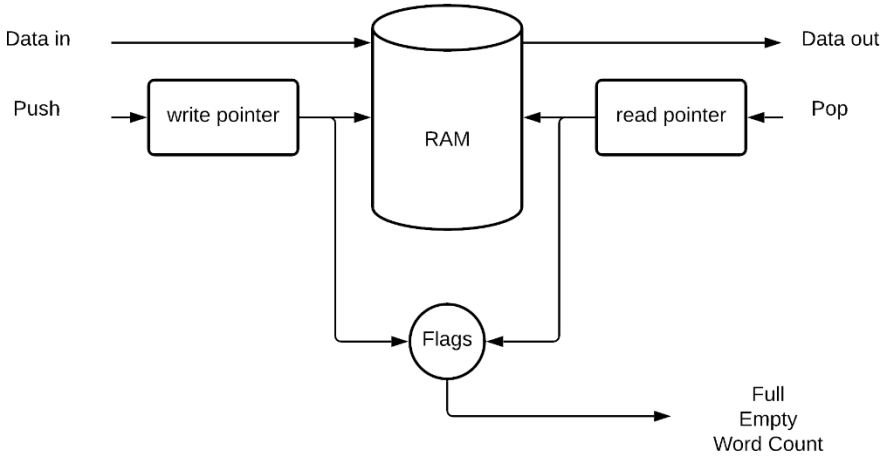

Trigger Setup - hw_ila_1
Capture Setup - hw_ila_1
Name
Operator
Radix
Value
Port
amplitude_valid
==
[B]
1
probe1[0]

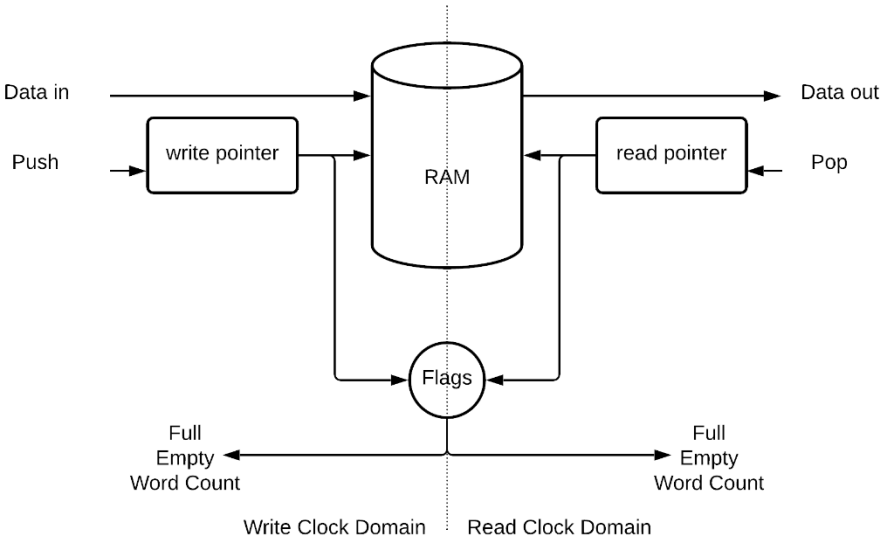

Tools
Reports
Window
Layout
View
Help
Create and Package New IP...
Create Interface Definition...
Enable Dynamic Function eXchange...
Run Tcl Script...
Property Editor
Ctrl+J
Associate ELF Files...
Generate Memory Configuration File...
Compile Simulation Libraries...
XHub Stores...
Custom Commands
Launch Vitis IDE
Language Templates
Settings...

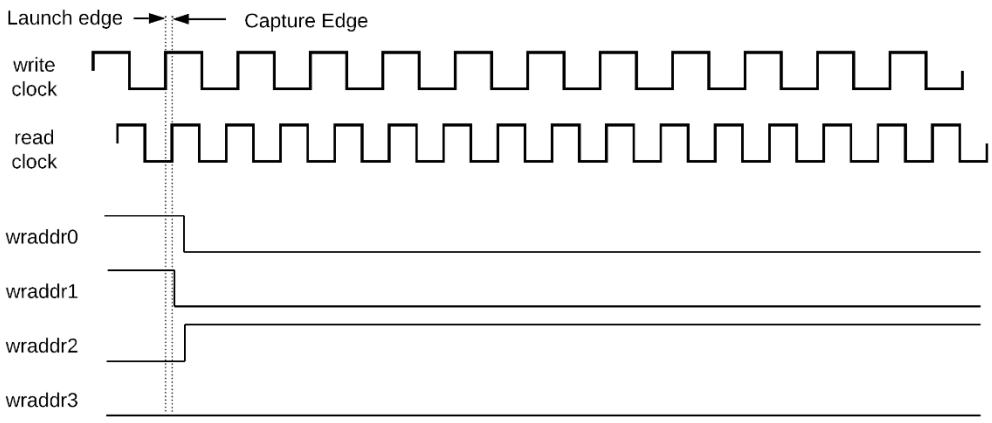

Address
Write Data
Clock
Read Data
Single Port
Write Clock
Write Data
Write Address
Read Clock
Read Address
Read Data
Simple Dual Port
Clock A
Write Data A
Address A
Clock B
Write Data B
Address B
Read Data A
Read Data B
True Dual Port

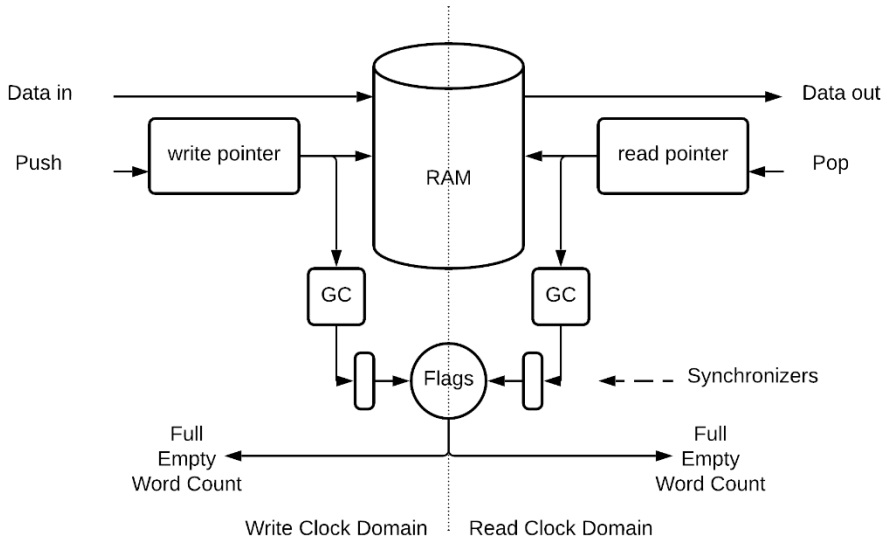

tHD:STA
tHIGH
clk
tLOW
tSU:STO
sda
tSU:DAT
tHD:DAT

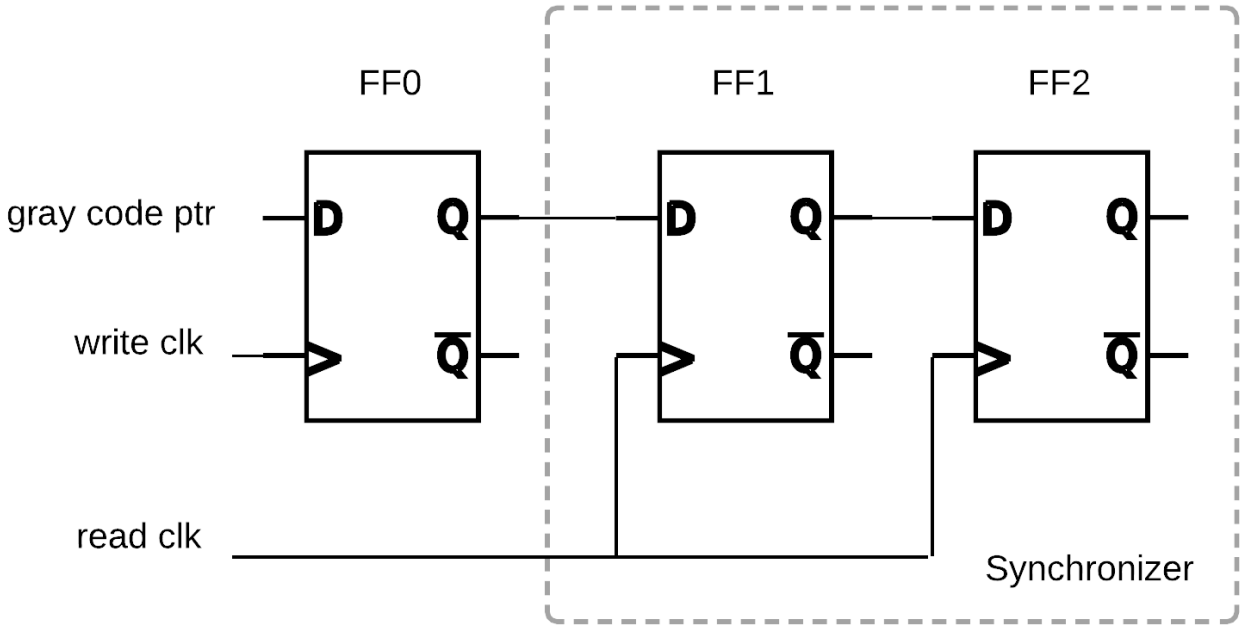

16 location FIFO
+
-
Accumulator
16 second average

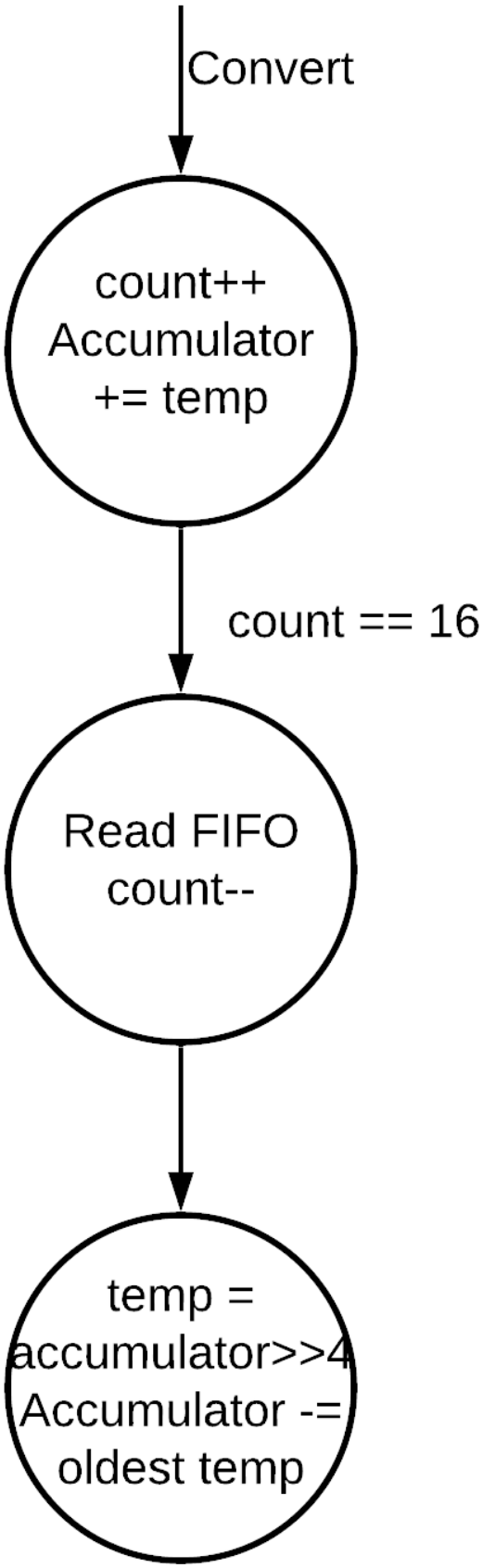

Data in
Data out
Push
write pointer
RAM
read pointer
Pop
Flags
Full
Empty
Word Count


Data in
Data out
Push
write pointer
RAM
read pointer
Pop
Flags
Full
Empty
Word Count
Full
Empty
Word Count
Write Clock Domain
Read Clock Domain

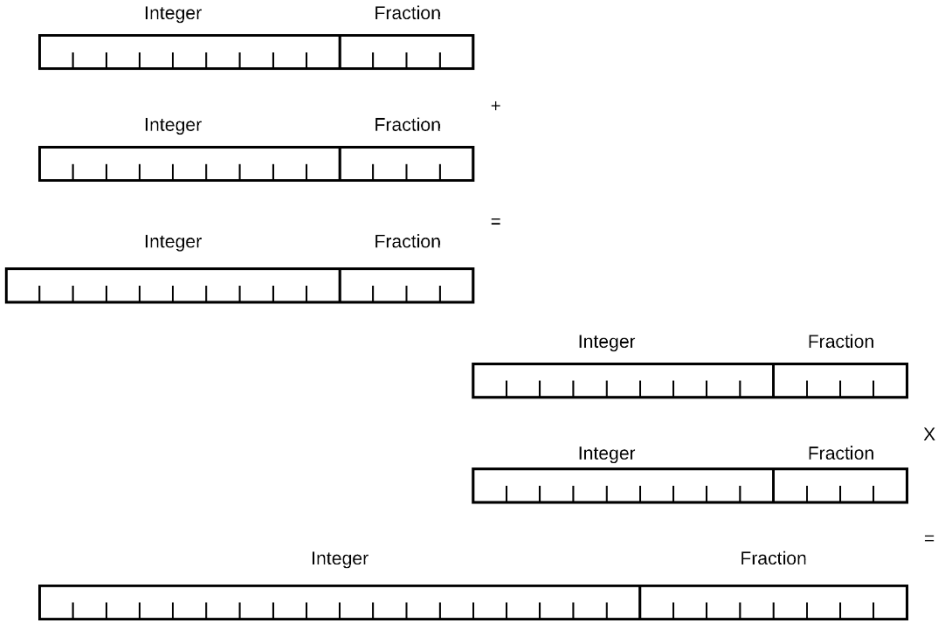

Launch edge
Capture Edge
write clock
read clock
wraddr0
wraddr1
wraddr2
wraddr3

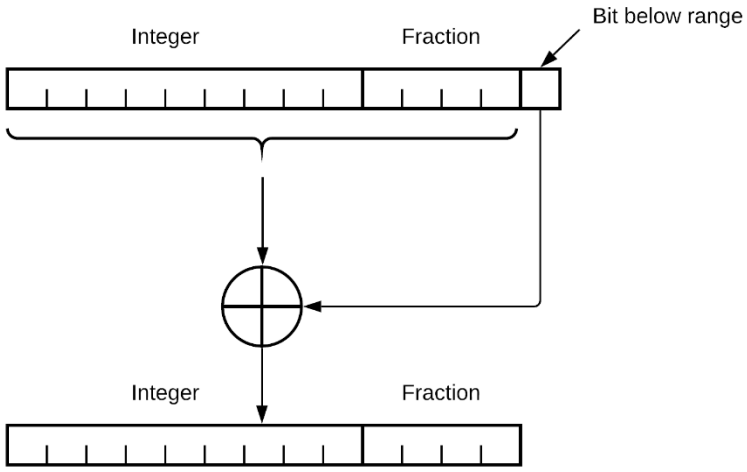

Data in
Push
write pointer
RAM
read pointer
Pop
Data out
GC
GC
Flags
Synchronizers
Full
Empty
Word Count
Full
Empty
Word Count
Write Clock Domain
Read Clock Domain


FF0
FF1
FF2
gray code ptr
write clk
read clk
D
Q
D
Q
D
Q
Q
Q
Q
Synchronizer

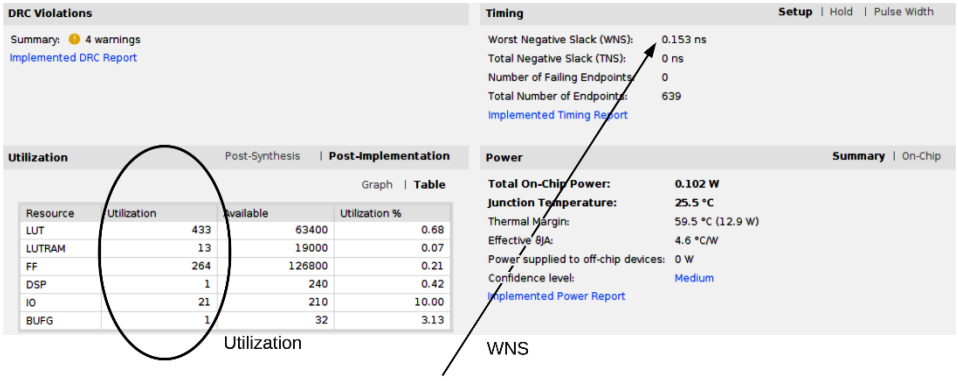

Convert
count++
Accumulator
+= temp
count == 16
Read FIFO
count--
temp =
accumulator>>4
Accumulator -=
oldest temp

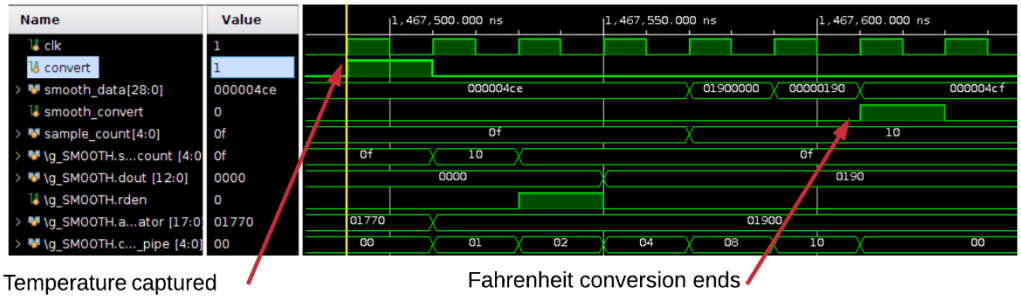
Chapter 6: Math, Parallelism, and Pipelined Design

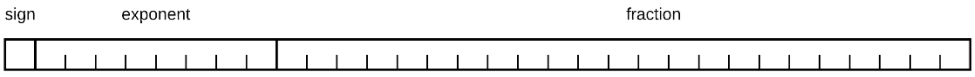


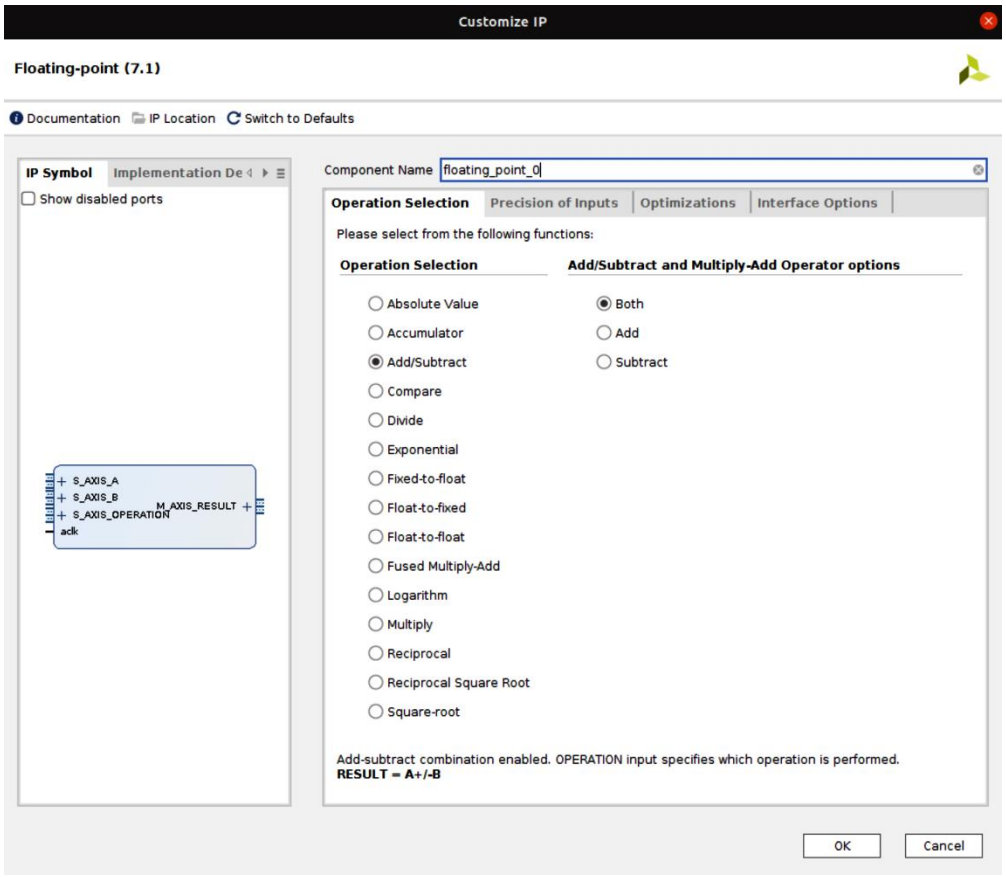


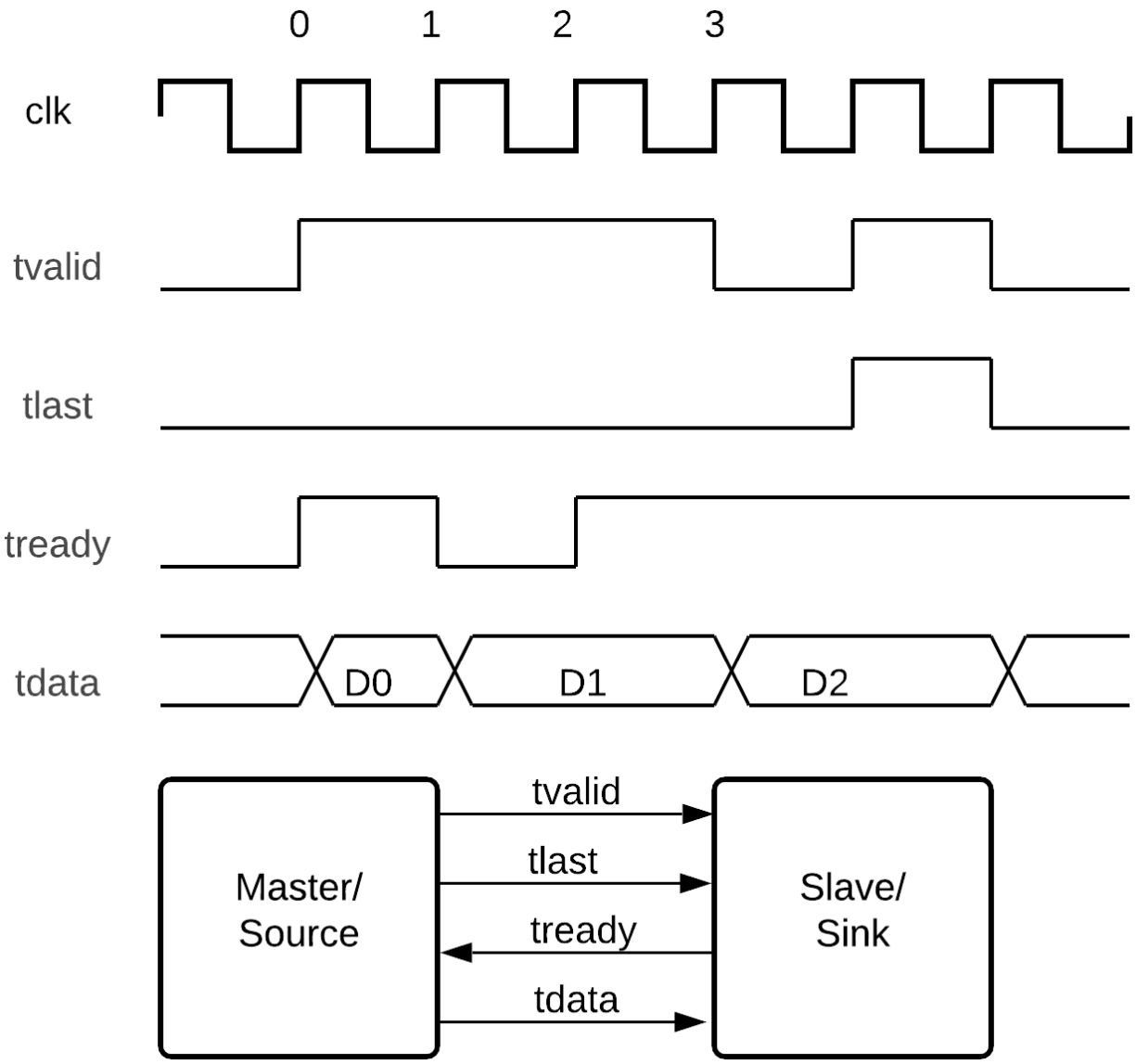
$$T_{Fahrenheit} = \left(T_{Celsius} \; x \; \frac{9}{5}\right) + \; 32$$

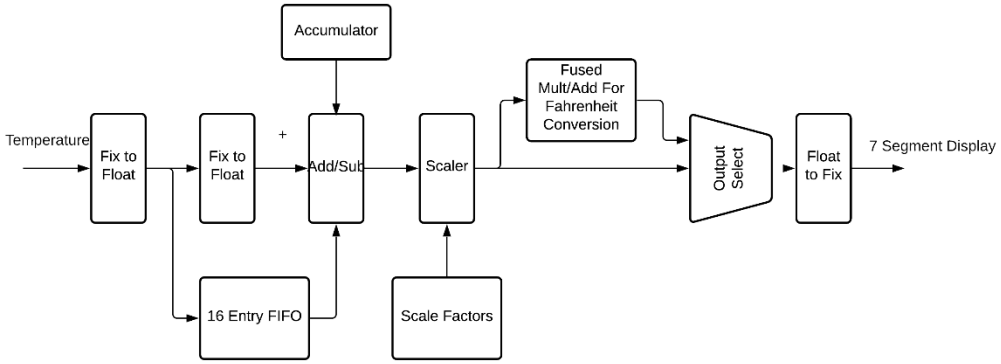

DRC Violations
Summary: 4 warnings
Implemented DRC Report
Timing
Setup | Hold | Pulse Width
Worst Negative Slack (WNS): 0.153 ns
Total Negative Slack (TNS): 0 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 639
Implemented Timing Report
Utilization
Post-Synthesis | Post-Implementation
Graph | Table
Resource | Utilization | Available | Utilization %
LUT | 433 | 63400 | 0.68
LUTRAM | 13 | 19000 | 0.07
FF | 264 | 126800 | 0.21
DSP | 1 | 240 | 0.42
IO | 21 | 210 | 10.00
BUFG | 1 | 32 | 3.13
Power
Summary | On-Chip
Total On-Chip Power: 0.102 W
Junction Temperature: 25.5 °C
Thermal Margin: 59.5 °C (12.9 W)
Effective θJA: 4.6 °C/W
Power supplied to off-chip devices: 0 W
Confidence level: Medium
Implemented Power Report
Utilization
WNS


Name
Value
clk
convert
smooth_data[28:0]
smooth_convert
sample_count[4:0]
\g_SMOOTH.s...count [4:0]
\g_SMOOTH.dout [12:0]
\g_SMOOTH.rden
\g_SMOOTH.a...ator [17:0]
\g_SMOOTH.c..._pipe [4:0]
1
1
000004ce
0
0f
0f
0000
0
01770
00
1,467,500.000 ns
1,467,550.000 ns
1,467,600.000 ns
000004ce
01900000
00000190
000004cf
0f
10
0f
10
0f
0000
0190
01770
01900
00
01
02
04
08
10
00
Temperature captured
Fahrenheit conversion ends


sign
exponent
fraction

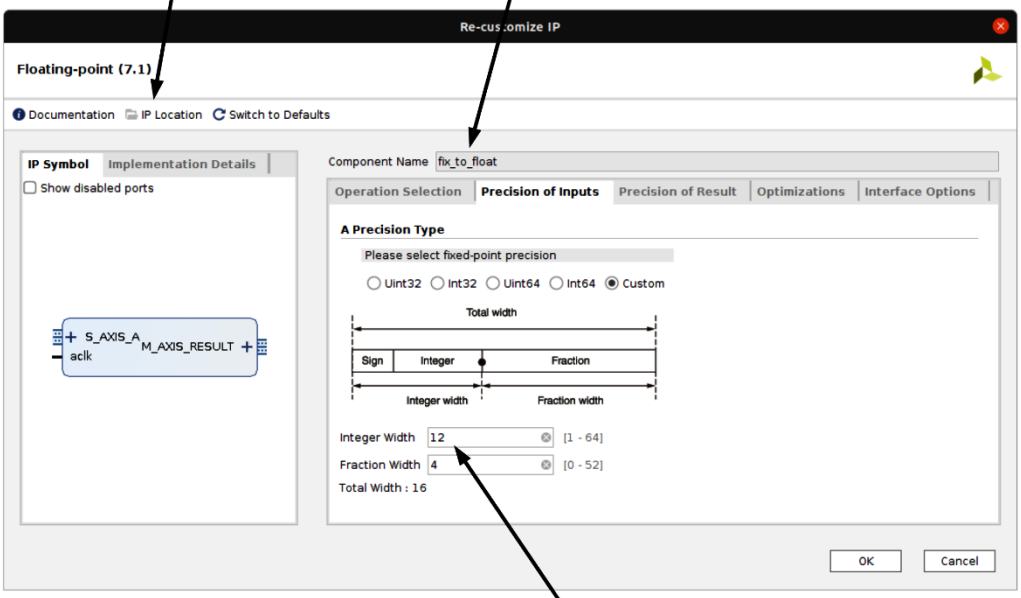

Customize IP
Floating-point (7.1)
Documentation
IP Location
Switch to Defaults
IP Symbol
Implementation De
Show disabled ports
S_AXIS_A
S_AXIS_B
S_AXIS_OPERATION
aclk
M_AXIS_RESULT
Component Name
floating_point_0
Operation Selection
Precision of Inputs
Optimizations
Interface Options
Please select from the following functions:
Operation Selection
Add/Subtract and Multiply-Add Operator options
Absolute Value
Accumulator
Add/Subtract
Compare
Divide
Exponential
Fixed-to-float
Float-to-fixed
Float-to-float
Fused Multiply-Add
Logarithm
Multiply
Reciprocal
Reciprocal Square Root
Square-root
Both
Add
Subtract
Add-subtract combination enabled. OPERATION input specifies which operation is performed.
RESULT = A+/-B
OK
Cancel


0
1
2
3
clk
tvalid
tlast
tready
tdata
D0
D1
D2
Master/
Source
tvalid
tlast
tready
tdata
Slave/
Sink

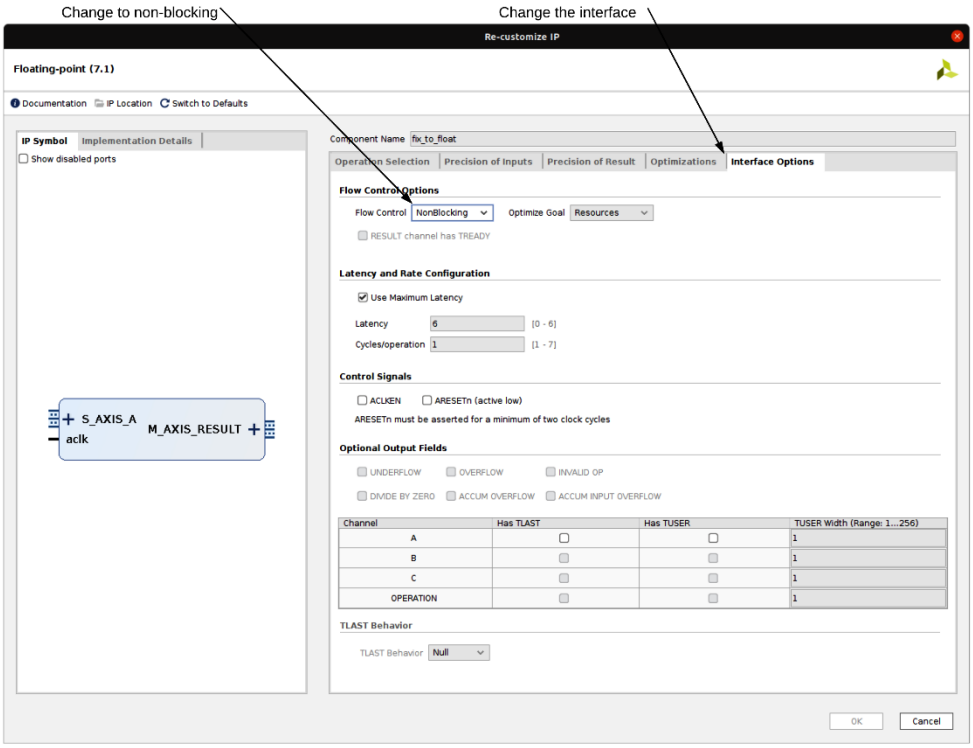


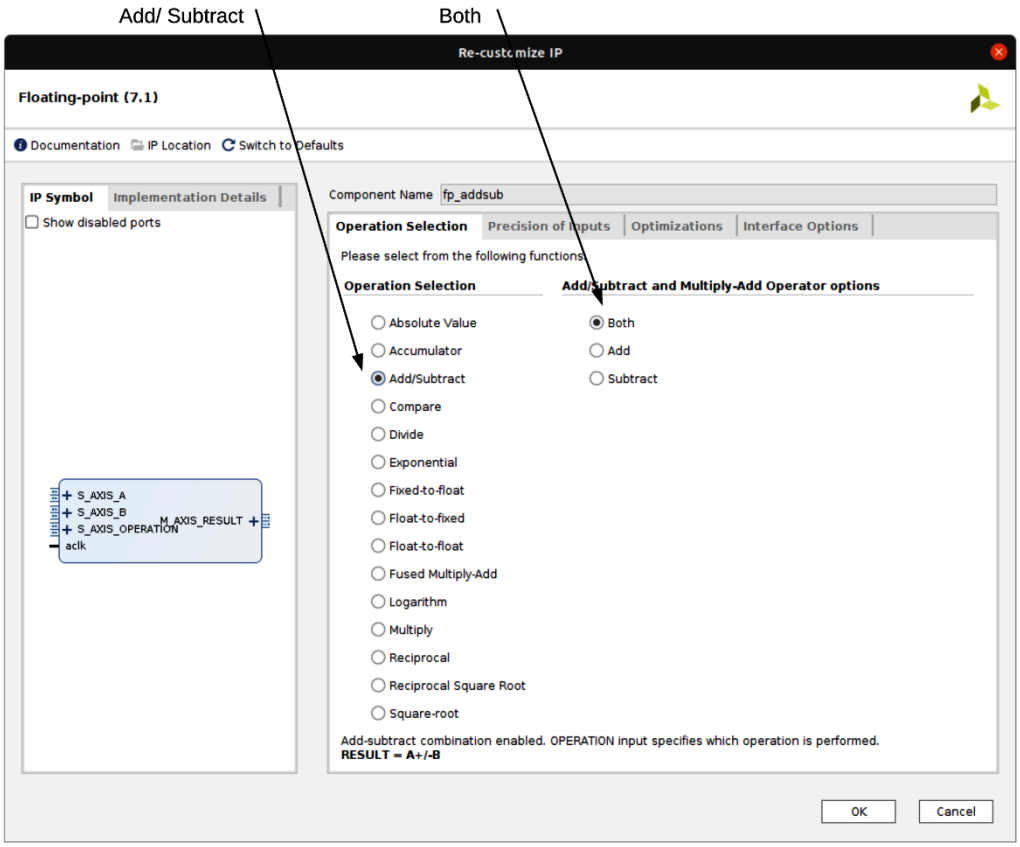
Set location to build/IP

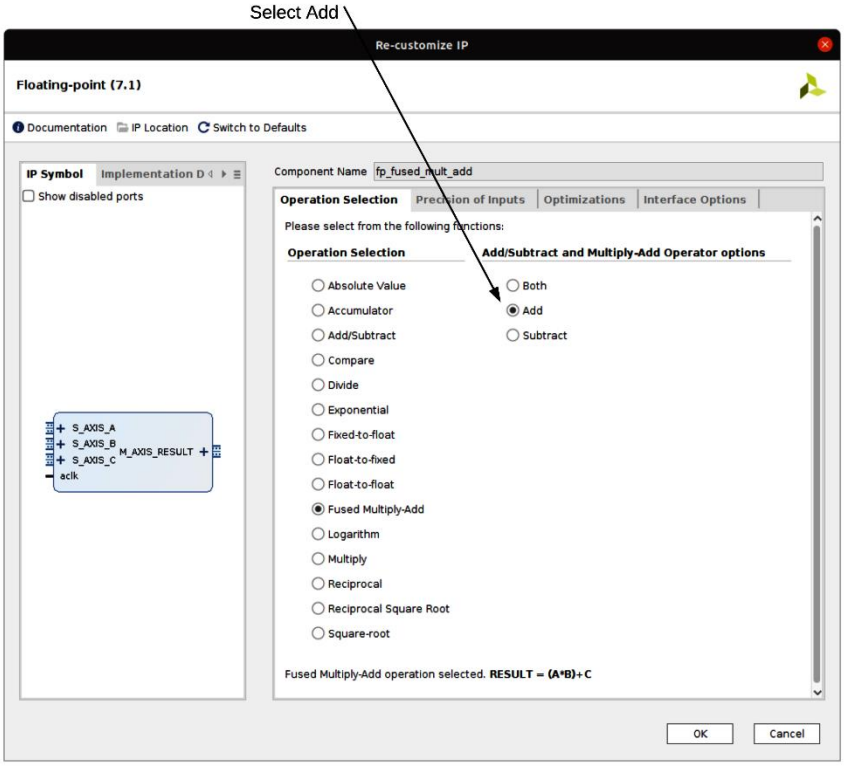
Rename

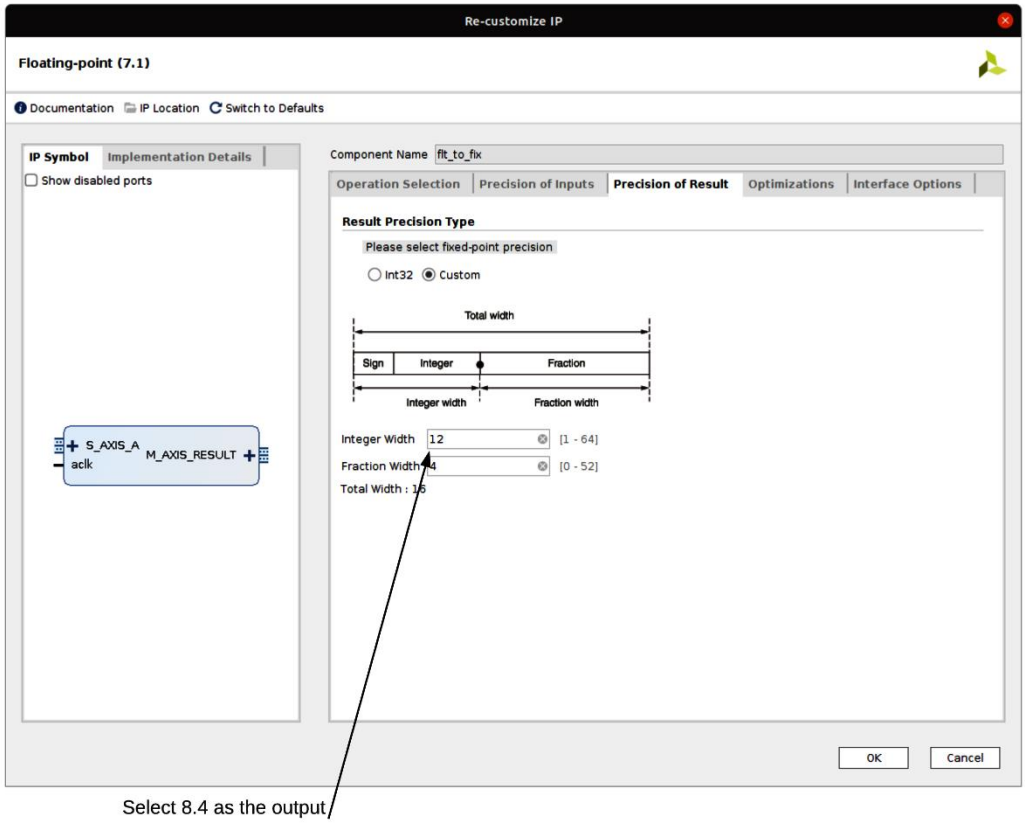


Format for our temperature sensor

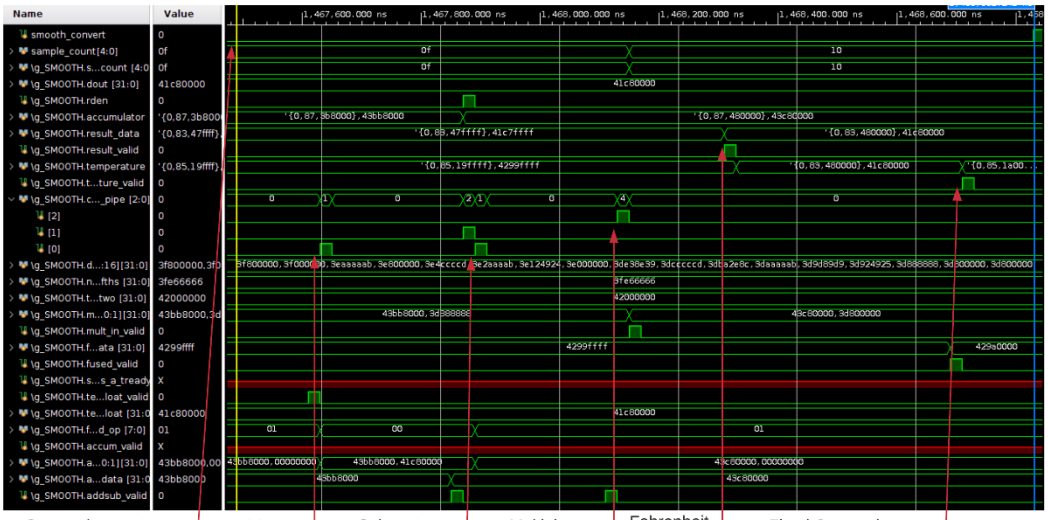

Change to non-blocking
Change the interface
Re-customize IP
Floating-point (7.1)
Documentation
IP Location
Switch to Defaults
IP Symbol
Implementation Details
Show disabled ports
S_AXIS_A
aclk
M_AXIS_RESULT
Component Name
fix_to_float
Operation Selection
Precision of Inputs
Precision of Result
Optimizations
Interface Options
Flow Control Options
Flow Control
NonBlocking
Optimize Goal
Resources
RESULT channel has TREADY
Latency and Rate Configuration
Use Maximum Latency
Latency
6
[0 - 6]
Cycles/operation
1
[1 - 7]
Control Signals
ACLKEN
ARESETn (active low)
ARESETn must be asserted for a minimum of two clock cycles
Optional Output Fields
UNDERFLOW
OVERFLOW
INVALID OP
DIVIDE BY ZERO
ACCUM OVERFLOW
ACCUM INPUT OVERFLOW
Channel
Has TLAST
Has TUSER
TUSER Width (Range: 1...256)
A
B
C
OPERATION
TLAST Behavior
TLAST Behavior
Null
OK
Cancel


Add/ Subtract
Both
Re-customize IP
Floating-point (7.1)
Documentation
IP Location
Switch to Defaults
IP Symbol
Implementation Details
Show disabled ports
S_AXIS_A
S_AXIS_B
S_AXIS_OPERATION
M_AXIS_RESULT
aclk
Component Name
fp_addsub
Operation Selection
Precision of Inputs
Optimizations
Interface Options
Please select from the following functions:
Operation Selection
Add/Subtract and Multiply-Add Operator options
Absolute Value
Accumulator
Add/Subtract
Compare
Divide
Exponential
Fixed-to-float
Float-to-fixed
Float-to-float
Fused Multiply-Add
Logarithm
Multiply
Reciprocal
Reciprocal Square Root
Square-root
Both
Add
Subtract
Add-subtract combination enabled. OPERATION input specifies which operation is performed.
RESULT = A+/-B
OK
Cancel

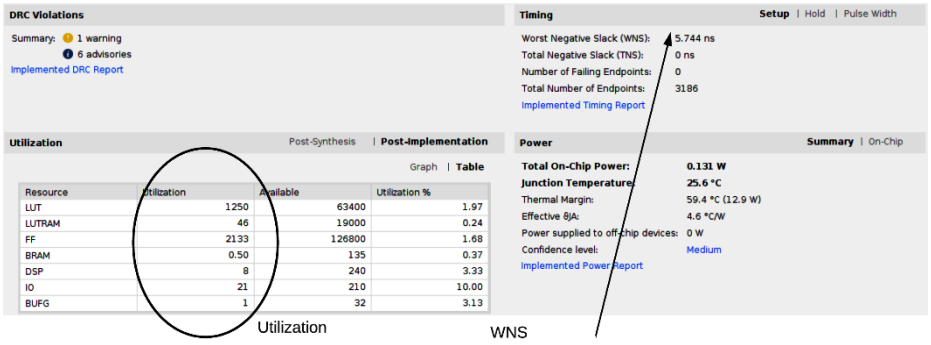

Select Add
Re-customize IP
Floating-point (7.1)
Documentation
IP Location
Switch to Defaults
IP Symbol
Implementation D
Show disabled ports
S_AXIS_A
S_AXIS_B
S_AXIS_C
M_AXIS_RESULT
aclk
Component Name
fp_fused_mult_add
Operation Selection
Precision of Inputs
Optimizations
Interface Options
Please select from the following functions:
Operation Selection
Add/Subtract and Multiply-Add Operator options
Absolute Value
Accumulator
Add/Subtract
Compare
Divide
Exponential
Fixed-to-float
Float-to-fixed
Float-to-float
Fused Multiply-Add
Logarithm
Multiply
Reciprocal
Reciprocal Square Root
Square-root
Both
Add
Subtract
Fused Multiply-Add operation selected. RESULT = (A*B)+C
OK
Cancel

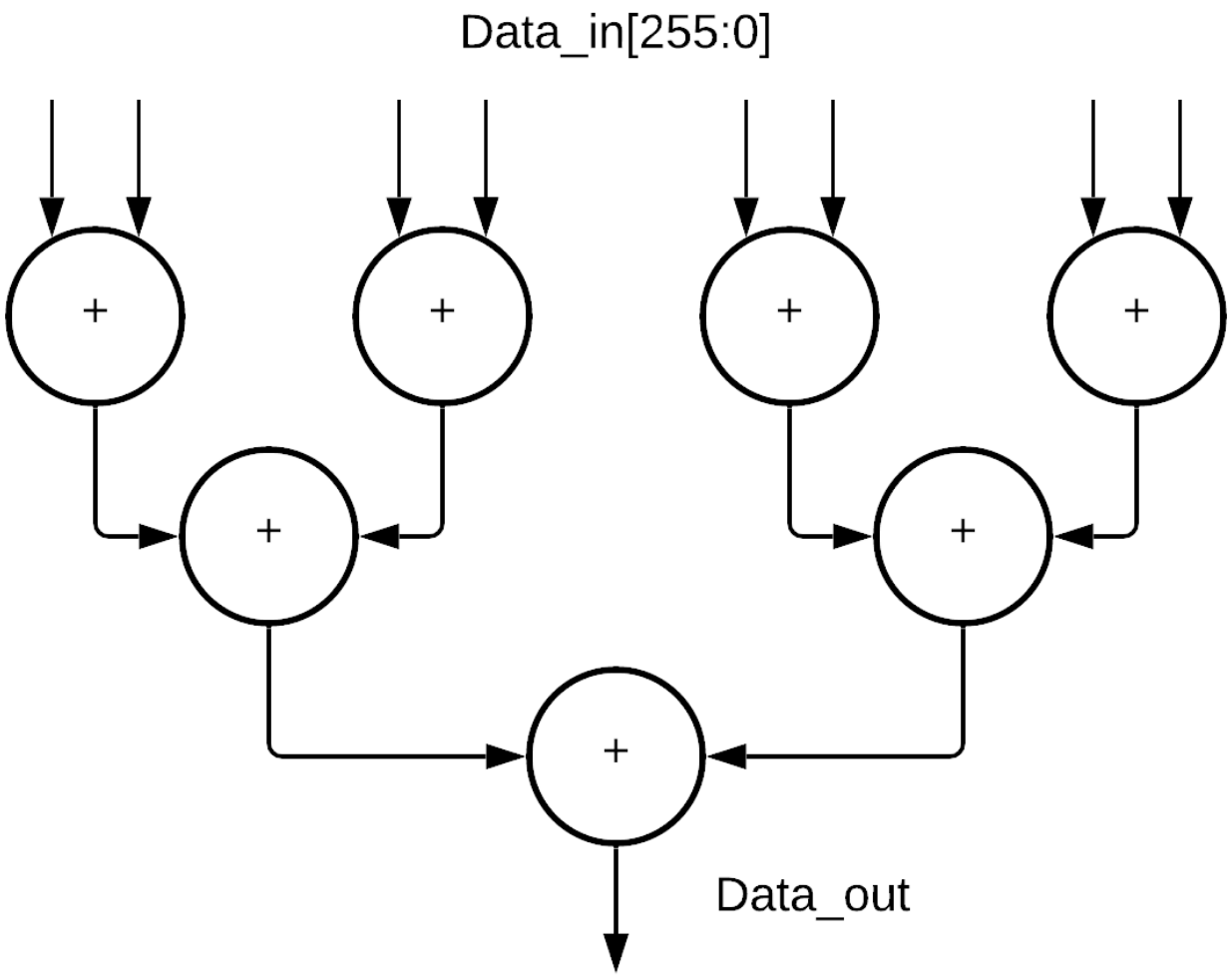


Select 8.4 as the output

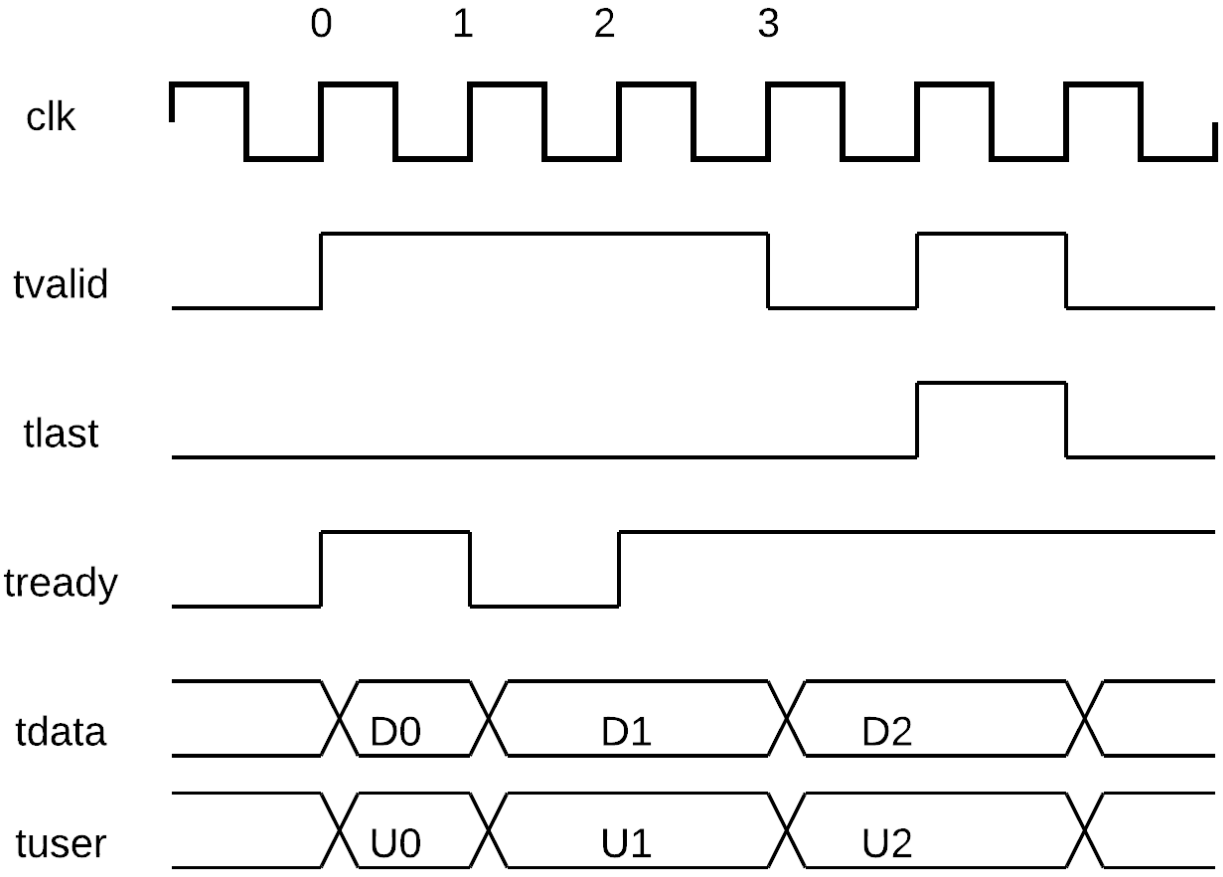


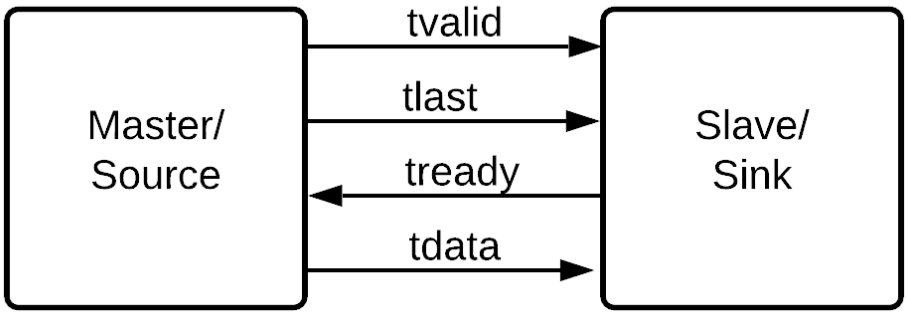
Conversion starts | Add start | Subtract start | Multiply start | Fahrenheit Conversion Starts | Fixed Conversion starts

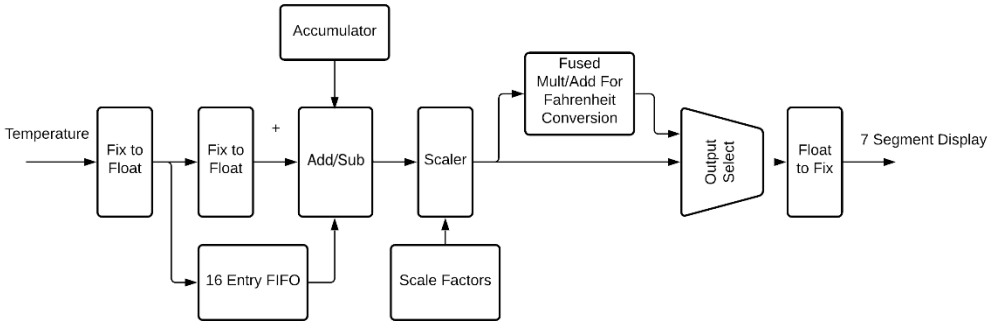

DRC Violations
Summary: 1 warning
6 advisories
Implemented DRC Report
Timing
Setup | Hold | Pulse Width
Worst Negative Slack (WNS): 5.744 ns
Total Negative Slack (TNS): 0 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 3186
Implemented Timing Report
Utilization
Post-Synthesis | Post-Implementation
Graph | Table
Resource | Utilization | Available | Utilization %
LUT | 1250 | 63400 | 1.97
LUTRAM | 46 | 19000 | 0.24
FF | 2133 | 126800 | 1.68
BRAM | 0.50 | 135 | 0.37
DSP | 8 | 240 | 3.33
IO | 21 | 210 | 10.00
BUFG | 1 | 32 | 3.13
Power
Summary | On-Chip
Total On-Chip Power: 0.131 W
Junction Temperature: 25.6 °C
Thermal Margin: 59.4 °C (12.9 W)
Effective θJA: 4.6 °C/W
Power supplied to off-chip devices: 0 W
Confidence level: Medium
Implemented Power Report
Utilization
WNS


Data_in[255:0]
Data_out

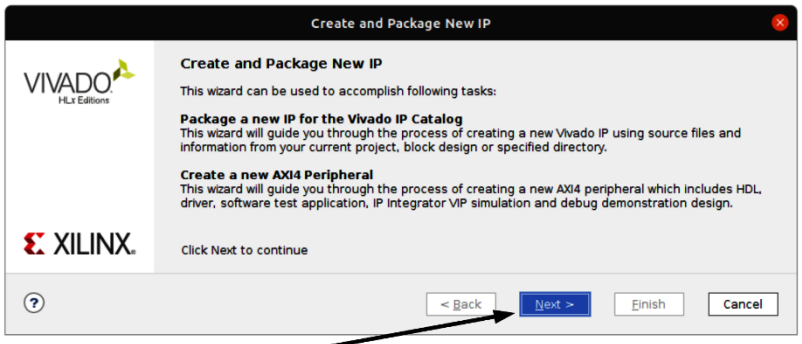
Chapter 7: Introduction to AXI



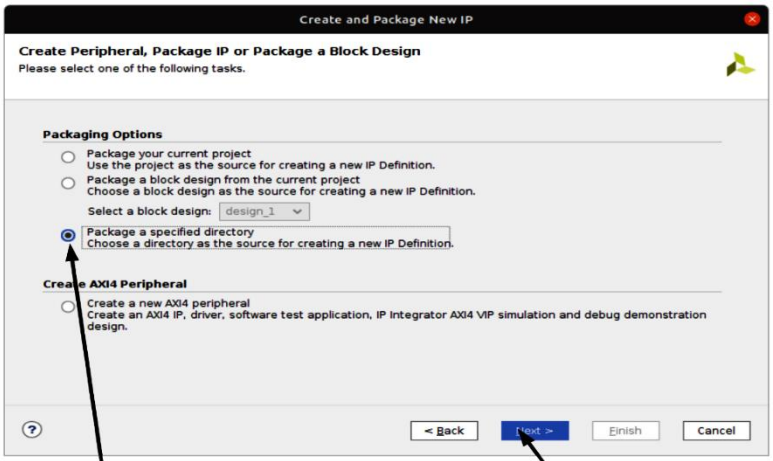




tools->Create and package IP

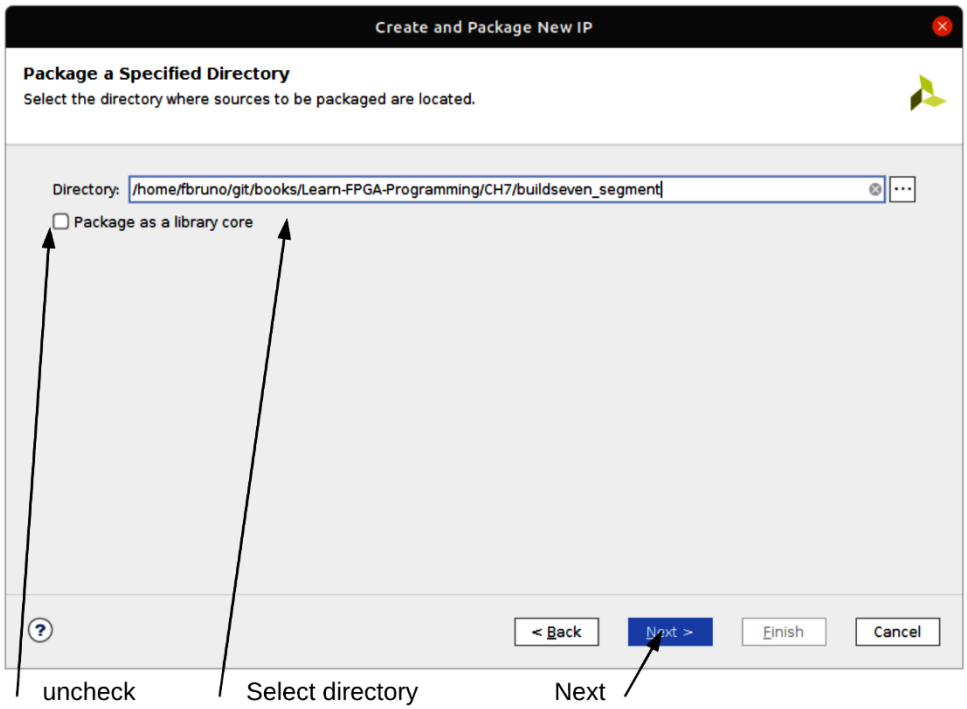


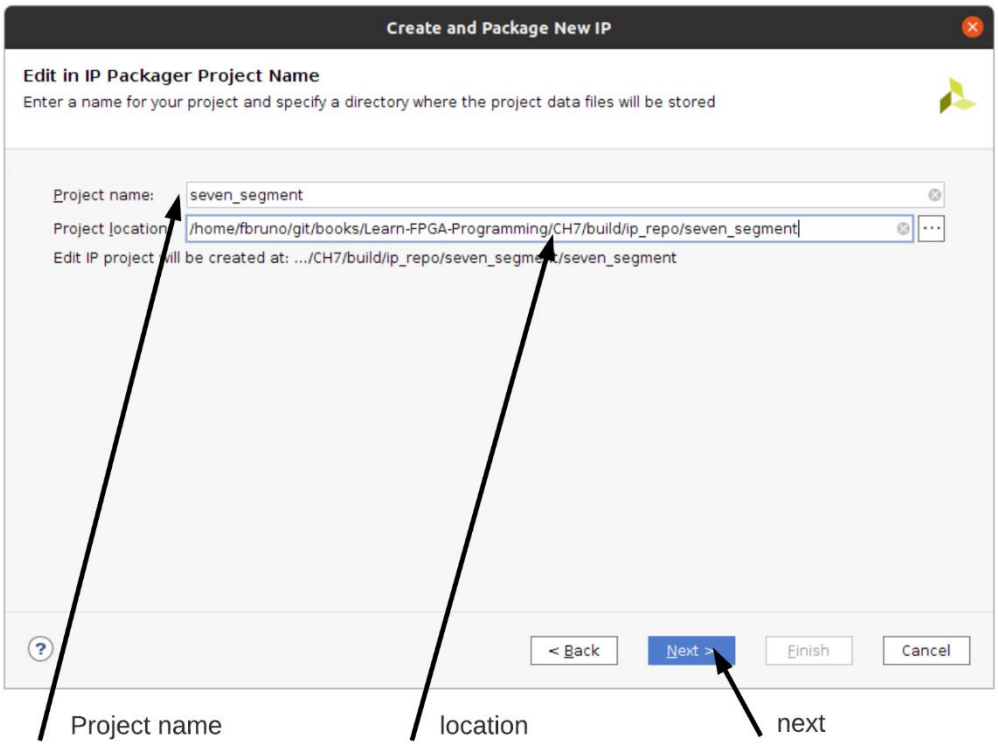
Next

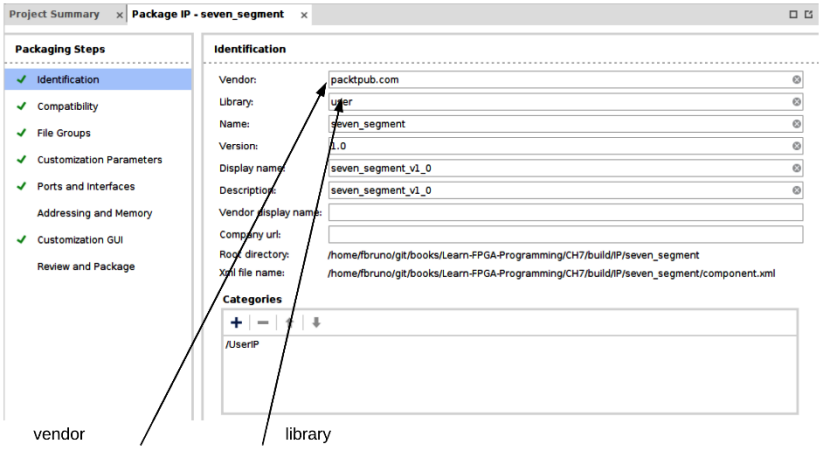


Package Directory

Continue

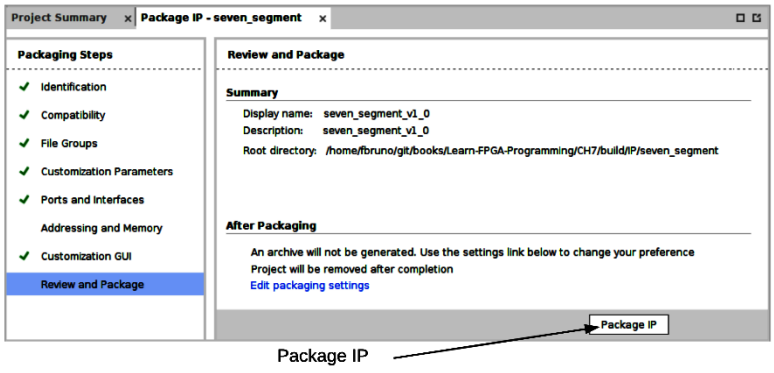

Create and Package New IP
Package a Specified Directory
Select the directory where sources to be packaged are located.
Directory:
/home/fbruno/git/books/Learn-FPGA-Programming/CH7/buildseven_segment
Package as a library core
< Back
Next >
Finish
Cancel
uncheck
Select directory
Next

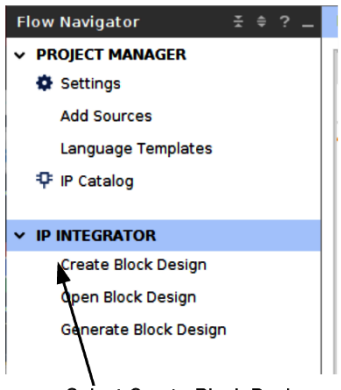

Create and Package New IP
Edit in IP Packager Project Name
Enter a name for your project and specify a directory where the project data files will be stored
Project name:
seven_segment
Project location:
/home/fbruno/git/books/Learn-FPGA-Programming/CH7/build/ip_repo/seven_segment
Edit IP project will be created at: .../CH7/build/ip_repo/seven_segment/seven_segment
< Back
Next >
Finish
Cancel
Project name
location
next

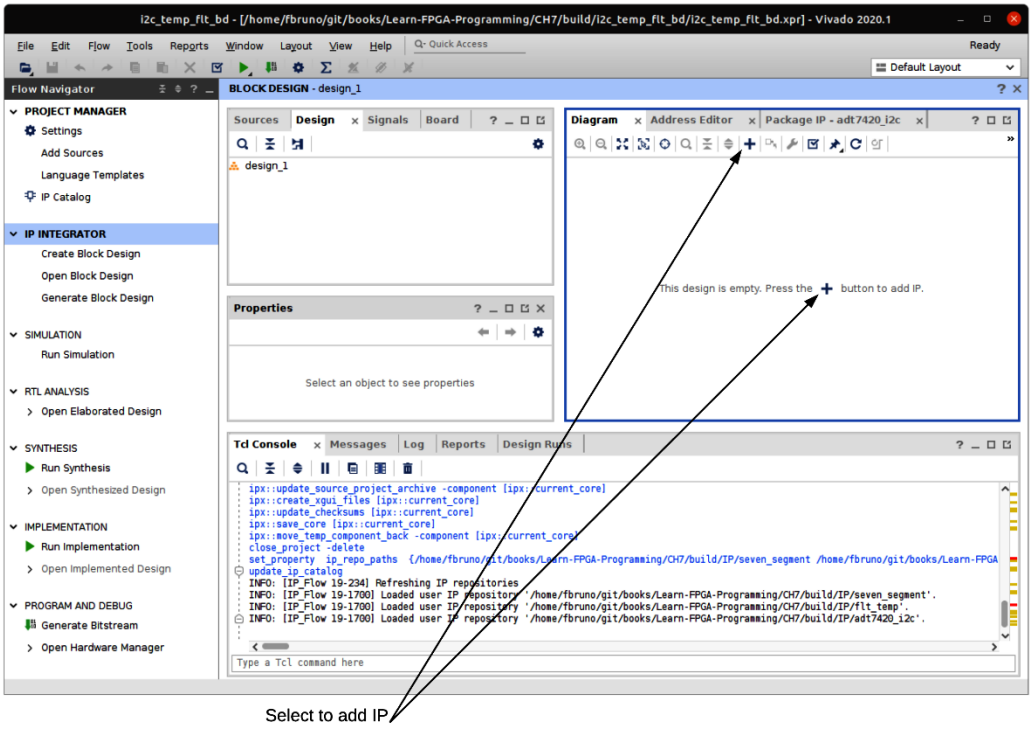


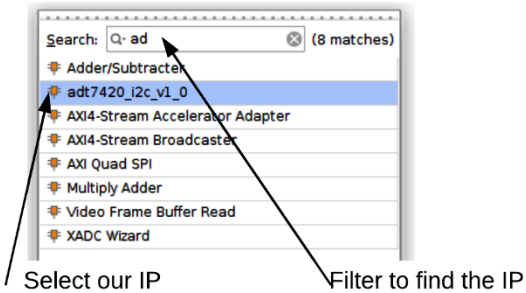
Ports and Interfaces

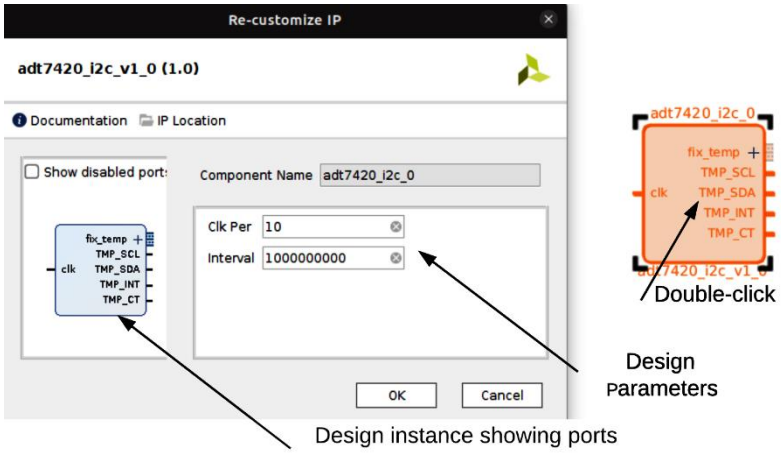
Name	Interface Mode	Enablement Dependency	Direction	Driver Value	Size Left	Size Right	Size Left Dependency	Size Right Dependency	Type Name
seven_segment	slave								
seven_segment_tdata			in	0	31	0	((NUM_SEGMENTS * 4)		wire
seven_segment_tuser			in	0	7	0	(NUM_SEGMENTS - 1)		wire
seven_segment_tvalid			in						wire
Clock and Reset Signals									
clk	slave								
anode			out		7	0	(NUM_SEGMENTS - 1)		logic
cathode			out		7	0			logic

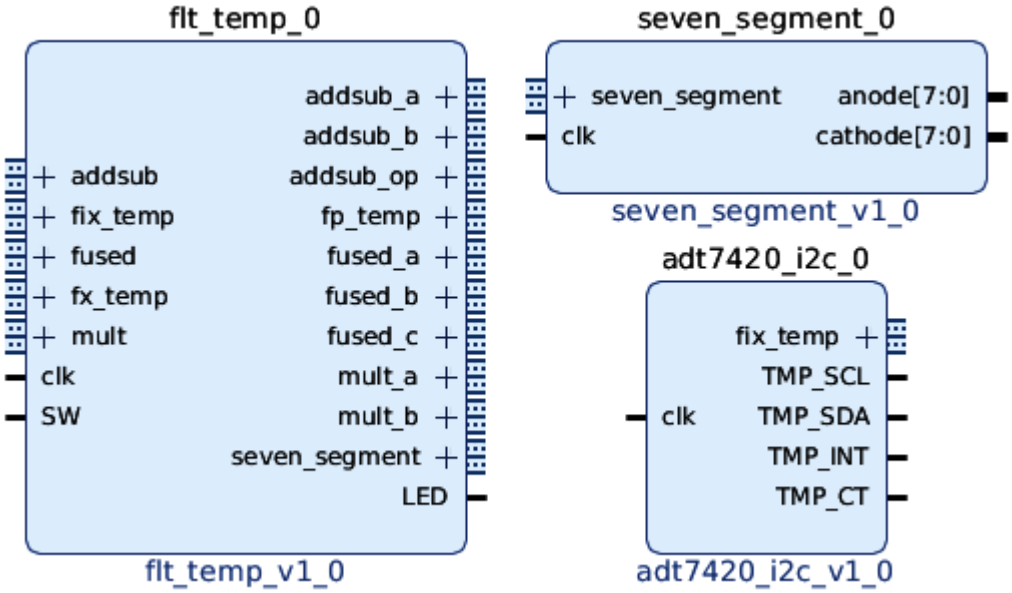


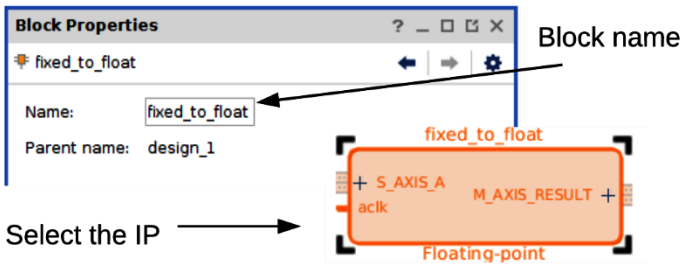

Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
Select Create Block Design

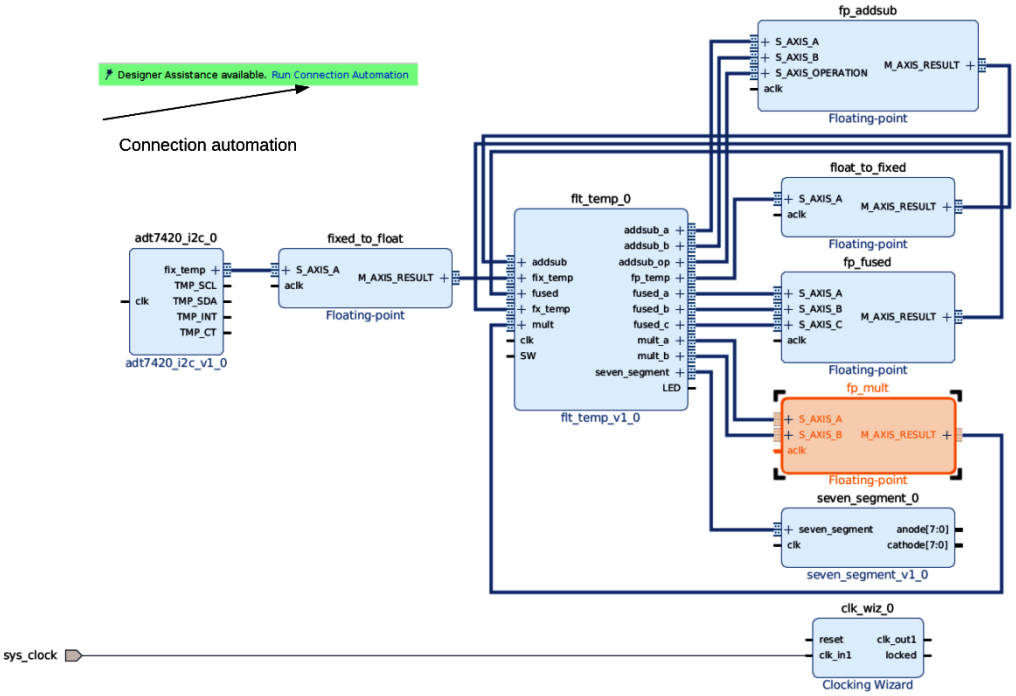

i2c_temp_flt_bd - [/home/fbruno/git/books/Learn-FPGA-Programming/CH7/build/i2c_temp_flt_bd/i2c_temp_flt_bd.xpr] - Vivado 2020.1
File Edit Flow Tools Reports Window Layout View Help
Ready
Default Layout
Flow Navigator
BLOCK DESIGN - design_1
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
Sources Design Signals Board
design_1
Diagram Address Editor Package IP - adt7420_i2c
This design is empty. Press the + button to add IP.
Properties
Select an object to see properties
Tcl Console Messages Log Reports Design Runs
ipx::update_source_project_archive -component [ipx::current_core]
ipx::create_xgui_files [ipx::current_core]
ipx::update_checksums [ipx::current_core]
ipx::save_core [ipx::current_core]
ipx::move_temp_component_back -component [ipx::current_core]
close_project -delete
set_property ip_repo_paths {/home/fbruno/git/books/Learn-FPGA-Programming/CH7/build/IP/seven_segment /home/fbruno/git/books/Learn-FPGA
update_ip_catalog
INFO: [IP_Flow 19-234] Refreshing IP repositories
INFO: [IP_Flow 19-1700] Loaded user IP repository '/home/fbruno/git/books/Learn-FPGA-Programming/CH7/build/IP/seven_segment'.
INFO: [IP_Flow 19-1700] Loaded user IP repository '/home/fbruno/git/books/Learn-FPGA-Programming/CH7/build/IP/flt_temp'.
INFO: [IP_Flow 19-1700] Loaded user IP repository '/home/fbruno/git/books/Learn-FPGA-Programming/CH7/build/IP/adt7420_i2c'.
Type a Tcl command here
Select to add IP

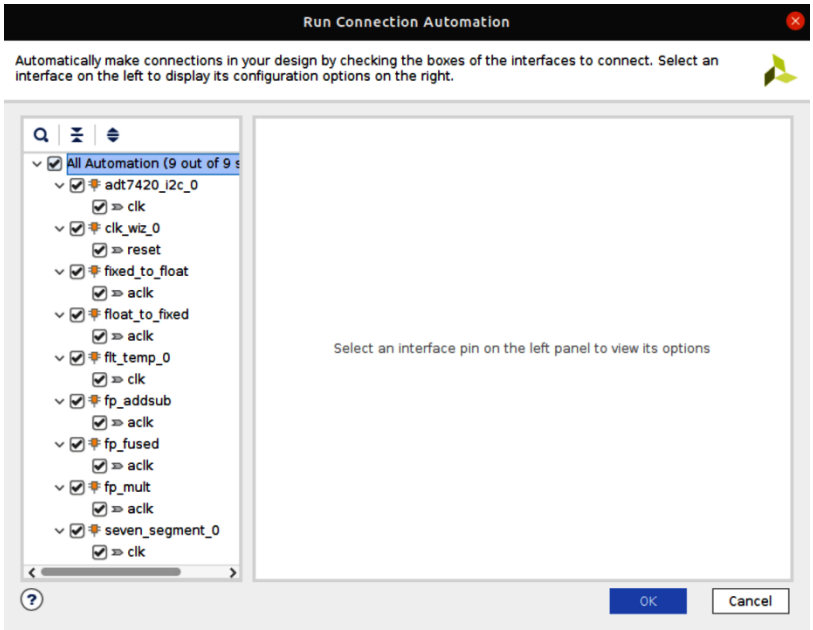

Search: ad
(8 matches)
Adder/Subtracter
adt7420_i2c_v1_0
AXI4-Stream Accelerator Adapter
AXI4-Stream Broadcaster
AXI Quad SPI
Multiply Adder
Video Frame Buffer Read
XADC Wizard
Select our IP
Filter to find the IP


Re-customize IP
adt7420_i2c_v1_0 (1.0)
Documentation
IP Location
Show disabled ports
Component Name
adt7420_i2c_0
Clk Per
10
Interval
1000000000
OK
Cancel
fix_temp
TMP_SCL
clk
TMP_SDA
TMP_INT
TMP_CT
adt7420_i2c_0
Double-click
Design Parameters
Design instance showing ports


flt_temp_0
addsub_a
addsub_b
addsub
addsub_op
fix_temp
fp_temp
fused
fused_a
fx_temp
fused_b
mult
fused_c
clk
mult_a
SW
mult_b
seven_segment
LED
flt_temp_v1_0
seven_segment_0
seven_segment
anode[7:0]
clk
cathode[7:0]
seven_segment_v1_0
adt7420_i2c_0
fix_temp
TMP_SCL
clk
TMP_SDA
TMP_INT
TMP_CT
adt7420_i2c_v1_0


Block Properties
fixed_to_float
Name:
fixed_to_float
Parent name:
design_1
Block name
Select the IP
fixed_to_float
S_AXIS_A
aclk
M_AXIS_RESULT
Floating-point


Designer Assistance available. Run Connection Automation
Connection automation
fp_addsub
S_AXIS_A
S_AXIS_B
S_AXIS_OPERATION
aclk
M_AXIS_RESULT
Floating-point
float_to_fixed
S_AXIS_A
aclk
M_AXIS_RESULT
Floating-point
flt_temp_0
addsub
fix_temp
fused
fx_temp
mult
clk
SW
addsub_a
addsub_b
addsub_op
fp_temp
fused_a
fused_b
fused_c
mult_a
mult_b
seven_segment
LED
flt_temp_v1_0
adt7420_i2c_0
fix_temp
TMP_SCL
clk
TMP_SDA
TMP_INT
TMP_CT
adt7420_i2c_v1_0
fixed_to_float
S_AXIS_A
aclk
M_AXIS_RESULT
Floating-point
fp_fused
S_AXIS_A
S_AXIS_B
S_AXIS_C
aclk
M_AXIS_RESULT
Floating-point
fp_mult
S_AXIS_A
S_AXIS_B
aclk
M_AXIS_RESULT
Floating-point
seven_segment_0
seven_segment
clk
anode[7:0]
cathode[7:0]
seven_segment_v1_0
clk_wiz_0
reset
clk_in1
clk_out1
locked
Clocking Wizard
sys_clock


Run Connection Automation
Automatically make connections in your design by checking the boxes of the interfaces to connect. Select an interface on the left to display its configuration options on the right.
All Automation (9 out of 9 s
adt7420_i2c_0
clk
clk_wiz_0
reset
fixed_to_float
aclk
float_to_fixed
aclk
flt_temp_0
clk
fp_addsub
aclk
fp_fused
aclk
fp_mult
aclk
seven_segment_0
clk
Select an interface pin on the left panel to view its options
OK
Cancel

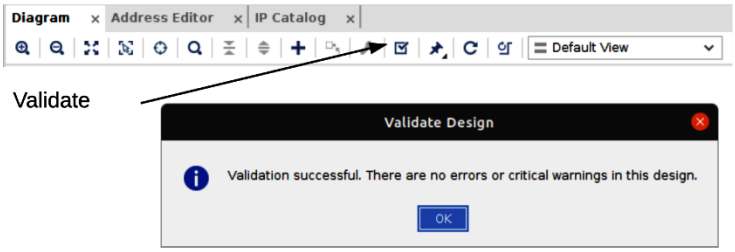
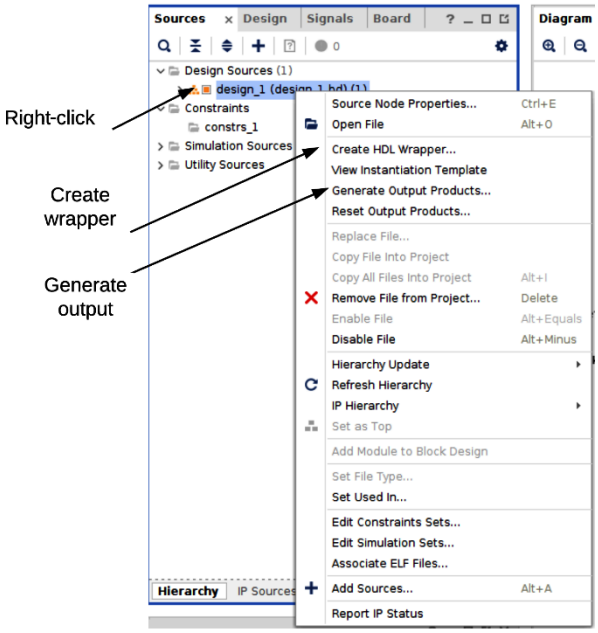
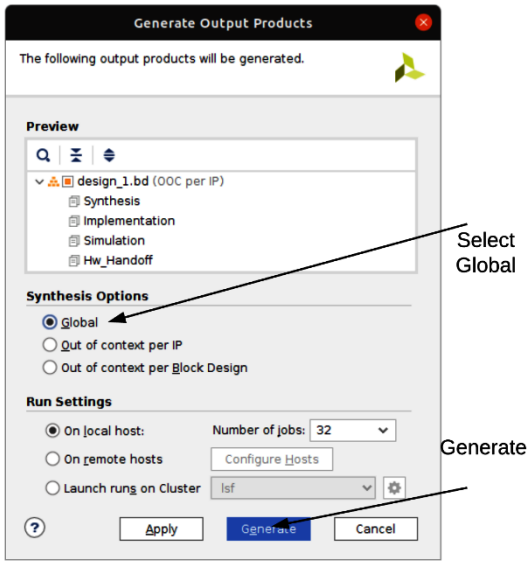
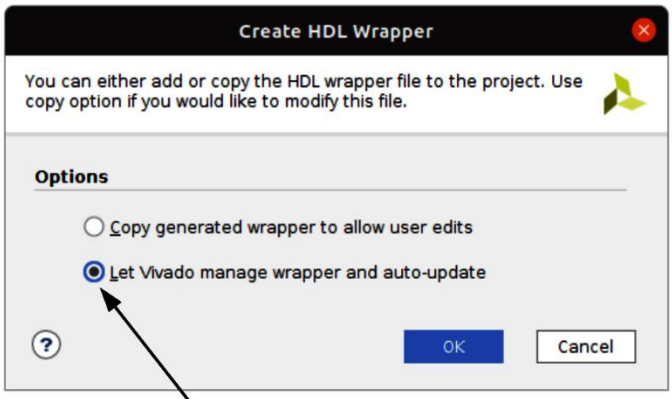
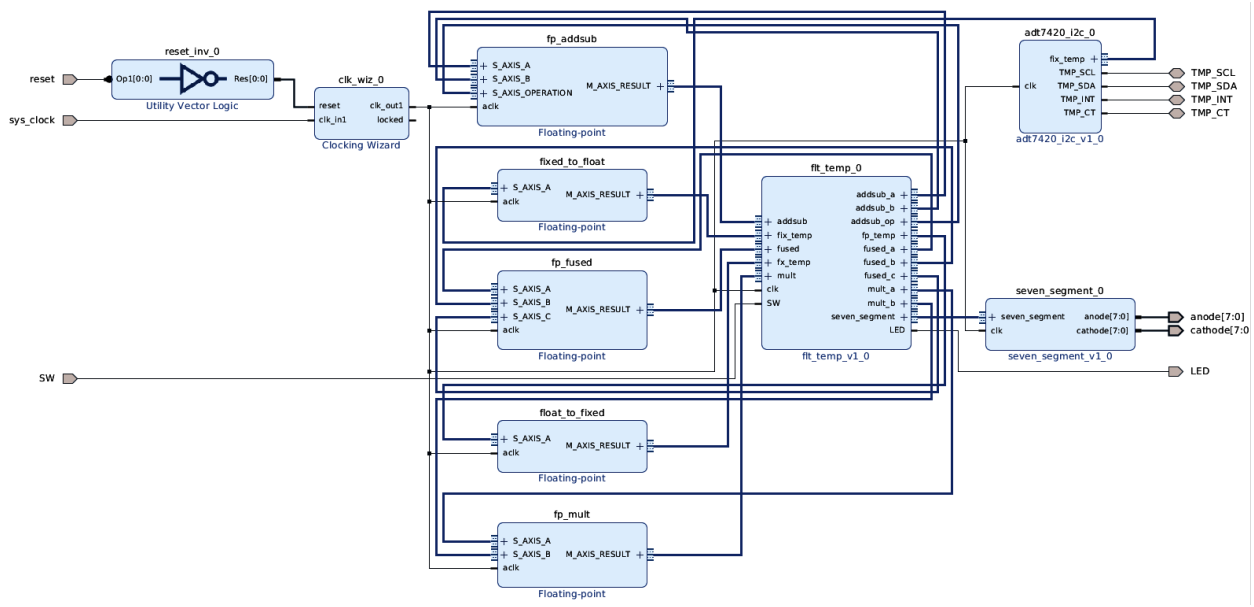


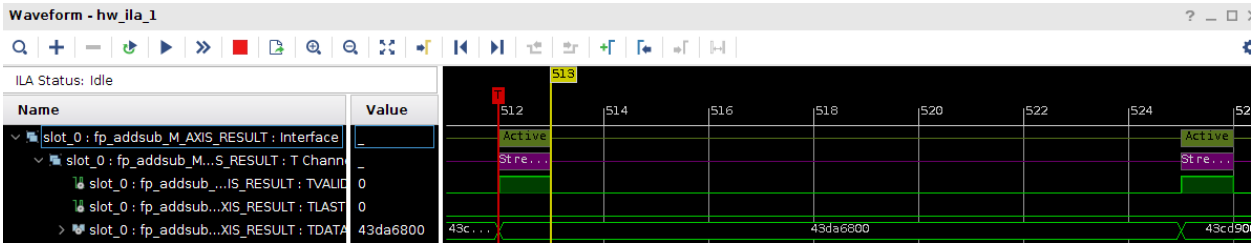
Diagram
Address Editor
IP Catalog
Default View
Validate
Validate Design
Validation successful. There are no errors or critical warnings in this design.
OK

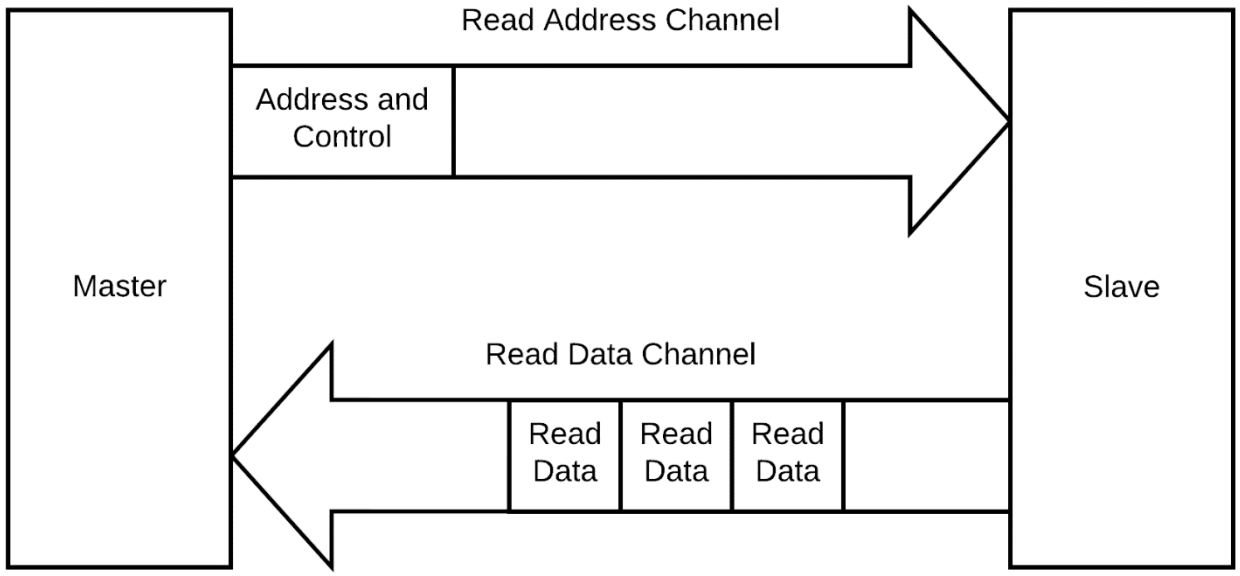

Sources
Design
Signals
Board
Diagram
Design Sources (1)
design_1 (design_1.bd) (1)
Constraints
constrs_1
Simulation Sources
Utility Sources
Right-click
Create wrapper
Generate output
Source Node Properties... Ctrl+E
Open File Alt+O
Create HDL Wrapper...
View Instantiation Template
Generate Output Products...
Reset Output Products...
Replace File...
Copy File Into Project
Copy All Files Into Project Alt+I
Remove File from Project... Delete
Enable File Alt+Equals
Disable File Alt+Minus
Hierarchy Update
Refresh Hierarchy
IP Hierarchy
Set as Top
Add Module to Block Design
Set File Type...
Set Used In...
Edit Constraints Sets...
Edit Simulation Sets...
Associate ELF Files...
Add Sources... Alt+A
Report IP Status
Hierarchy
IP Sources

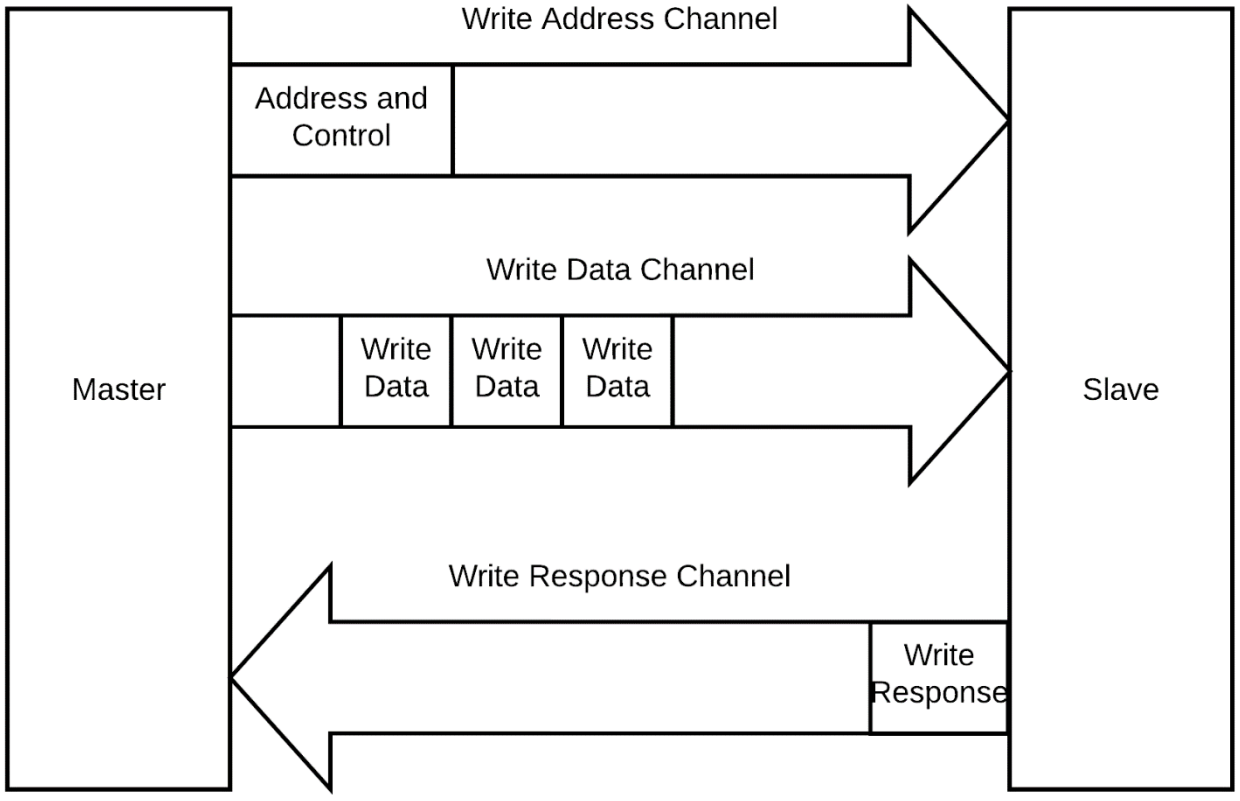

Generate Output Products
The following output products will be generated.
Preview
design_1.bd (OOC per IP)
Synthesis
Implementation
Simulation
Hw_Handoff
Synthesis Options
Global
Out of context per IP
Out of context per Block Design
Run Settings
On local host:
Number of jobs: 32
On remote hosts
Configure Hosts
Launch runs on Cluster
lsf
Apply
Generate
Cancel
Select Global
Generate

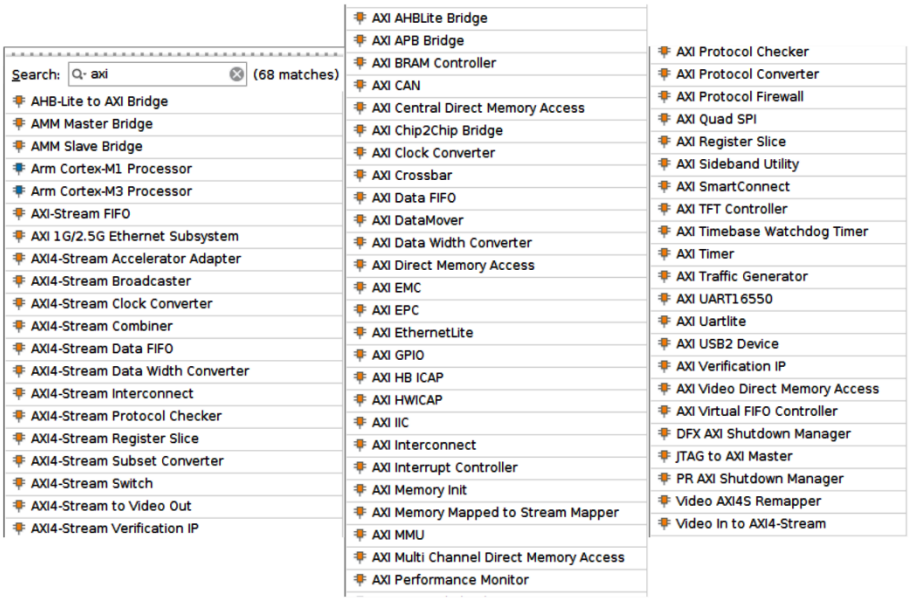

Create HDL Wrapper
You can either add or copy the HDL wrapper file to the project. Use copy option if you would like to modify this file.
Options
Copy generated wrapper to allow user edits
Let Vivado manage wrapper and auto-update
OK
Cancel
Let Vivado manage IP

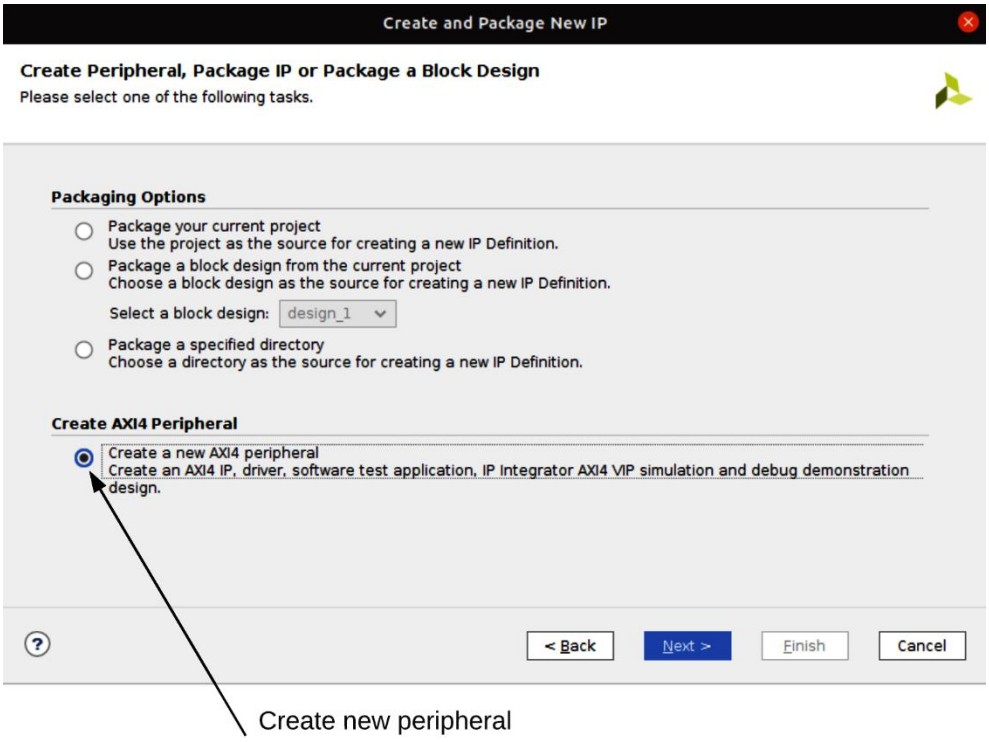

reset_inv_0
Utility Vector Logic
clk_wiz_0
Clocking Wizard
fp_addsub
Floating-point
fixed_to_float
Floating-point
fp_fused
Floating-point
float_to_fixed
Floating-point
fp_mult
Floating-point
flt_temp_0
flt_temp_v1_0
adt7420_i2c_0
adt7420_i2c_v1_0
seven_segment_0
seven_segment_v1_0
reset
sys_clock
SW
LED
TMP_SCL
TMP_SDA
TMP_INT
TMP_CT
anode[7:0]
cathode[7:0]

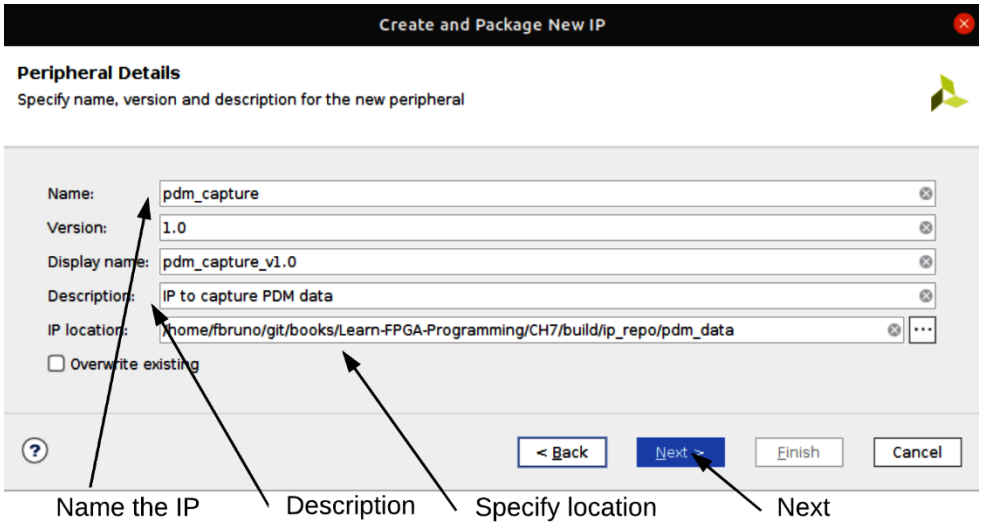

Waveform - hw_ila_1
ILA Status: Idle
Name
Value
slot_0 : fp_addsub_M_AXIS_RESULT : Interface
slot_0 : fp_addsub_M...S_RESULT : T Chann
slot_0 : fp_addsub_...IS_RESULT : TVALID
slot_0 : fp_addsub...XIS_RESULT : TLAST
slot_0 : fp_addsub...XIS_RESULT : TDATA
43da6800
513
512
514
516
518
520
522
524
Active
Stre...
43da6800

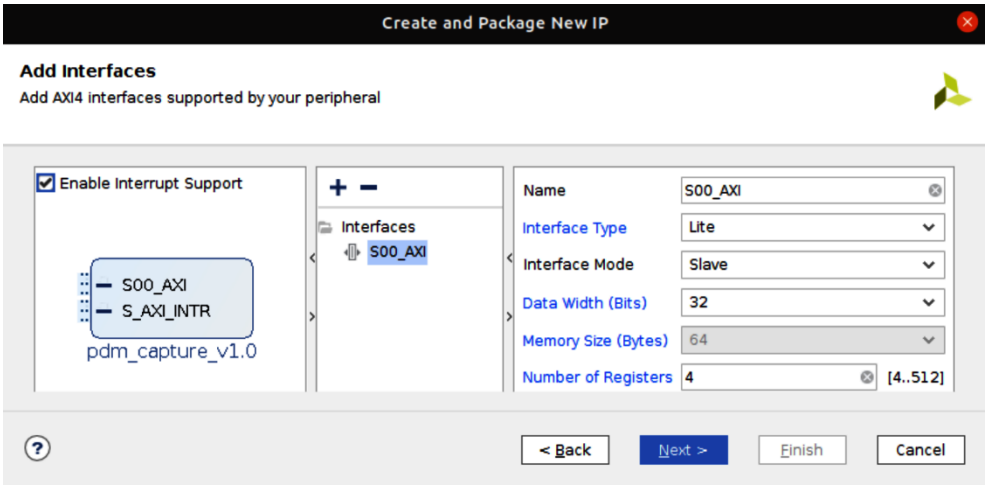

Read Address Channel
Address and Control
Master
Slave
Read Data Channel
Read Data
Read Data
Read Data

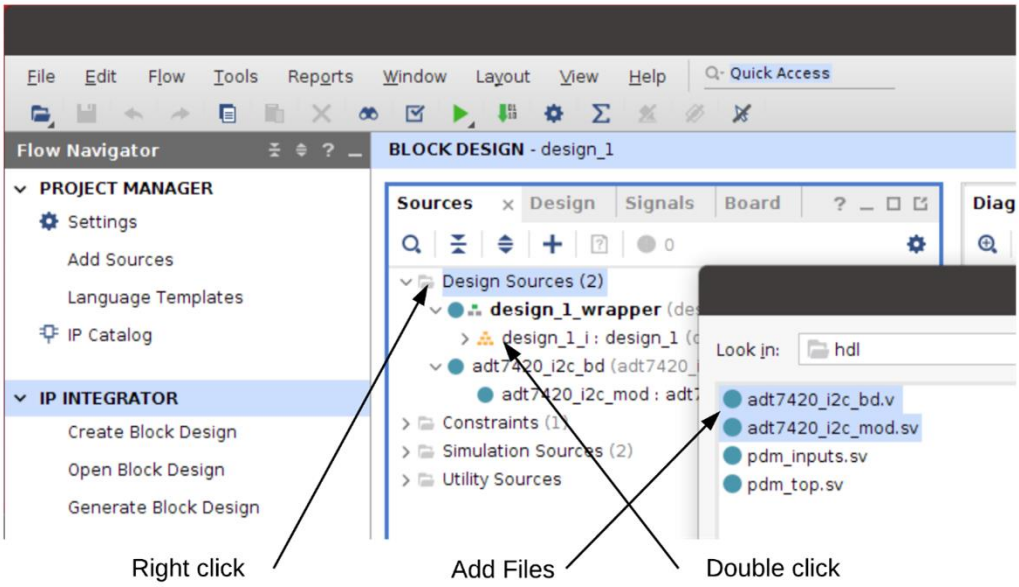

Write Address Channel
Address and Control
Write Data Channel
Master
Write Data
Write Data
Write Data
Slave
Write Response Channel
Write Response

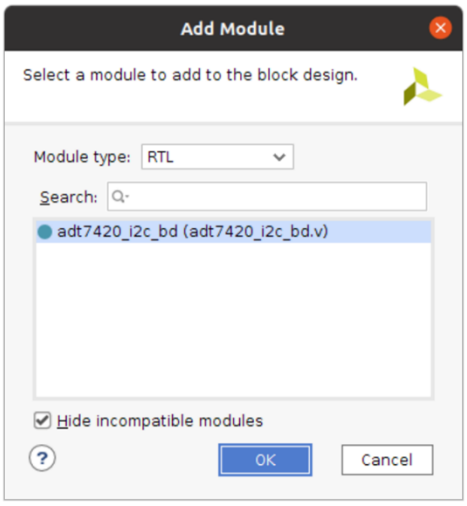

Search: axi (68 matches)
AHB-Lite to AXI Bridge
AMM Master Bridge
AMM Slave Bridge
Arm Cortex-M1 Processor
Arm Cortex-M3 Processor
AXI-Stream FIFO
AXI 1G/2.5G Ethernet Subsystem
AXI4-Stream Accelerator Adapter
AXI4-Stream Broadcaster
AXI4-Stream Clock Converter
AXI4-Stream Combiner
AXI4-Stream Data FIFO
AXI4-Stream Data Width Converter
AXI4-Stream Interconnect
AXI4-Stream Protocol Checker
AXI4-Stream Register Slice
AXI4-Stream Subset Converter
AXI4-Stream Switch
AXI4-Stream to Video Out
AXI4-Stream Verification IP
AXI AHBLite Bridge
AXI APB Bridge
AXI BRAM Controller
AXI CAN
AXI Central Direct Memory Access
AXI Chip2Chip Bridge
AXI Clock Converter
AXI Crossbar
AXI Data FIFO
AXI DataMover
AXI Data Width Converter
AXI Direct Memory Access
AXI EMC
AXI EPC
AXI EthernetLite
AXI GPIO
AXI HB ICAP
AXI HWICAP
AXI IIC
AXI Interconnect
AXI Interrupt Controller
AXI Memory Init
AXI Memory Mapped to Stream Mapper
AXI MMU
AXI Multi Channel Direct Memory Access
AXI Performance Monitor
AXI Protocol Checker
AXI Protocol Converter
AXI Protocol Firewall
AXI Quad SPI
AXI Register Slice
AXI Sideband Utility
AXI SmartConnect
AXI TFT Controller
AXI Timebase Watchdog Timer
AXI Timer
AXI Traffic Generator
AXI UART16550
AXI Uartlite
AXI USB2 Device
AXI Verification IP
AXI Video Direct Memory Access
AXI Virtual FIFO Controller
DFX AXI Shutdown Manager
JTAG to AXI Master
PR AXI Shutdown Manager
Video AXI4S Remapper
Video In to AXI4-Stream

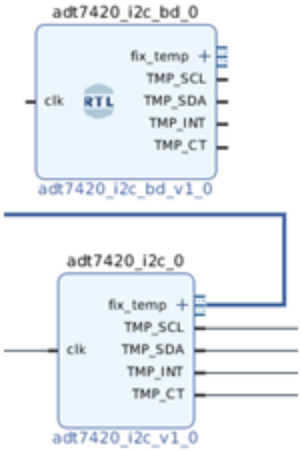

Create and Package New IP
Create Peripheral, Package IP or Package a Block Design
Please select one of the following tasks.
Packaging Options
Package your current project
Use the project as the source for creating a new IP Definition.
Package a block design from the current project
Choose a block design as the source for creating a new IP Definition.
Select a block design: design_1
Package a specified directory
Choose a directory as the source for creating a new IP Definition.
Create AXI4 Peripheral
Create a new AXI4 peripheral
Create an AXI4 IP, driver, software test application, IP Integrator AXI4 VIP simulation and debug demonstration design.
< Back
Next >
Finish
Cancel
Create new peripheral


Create and Package New IP
Peripheral Details
Specify name, version and description for the new peripheral
Name:
pdm_capture
Version:
1.0
Display name:
pdm_capture_v1.0
Description:
IP to capture PDM data
IP location:
/home/fbruno/git/books/Learn-FPGA-Programming/CH7/build/ip_repo/pdm_data
Overwrite existing
< Back
Next >
Finish
Cancel
Name the IP
Description
Specify location
Next

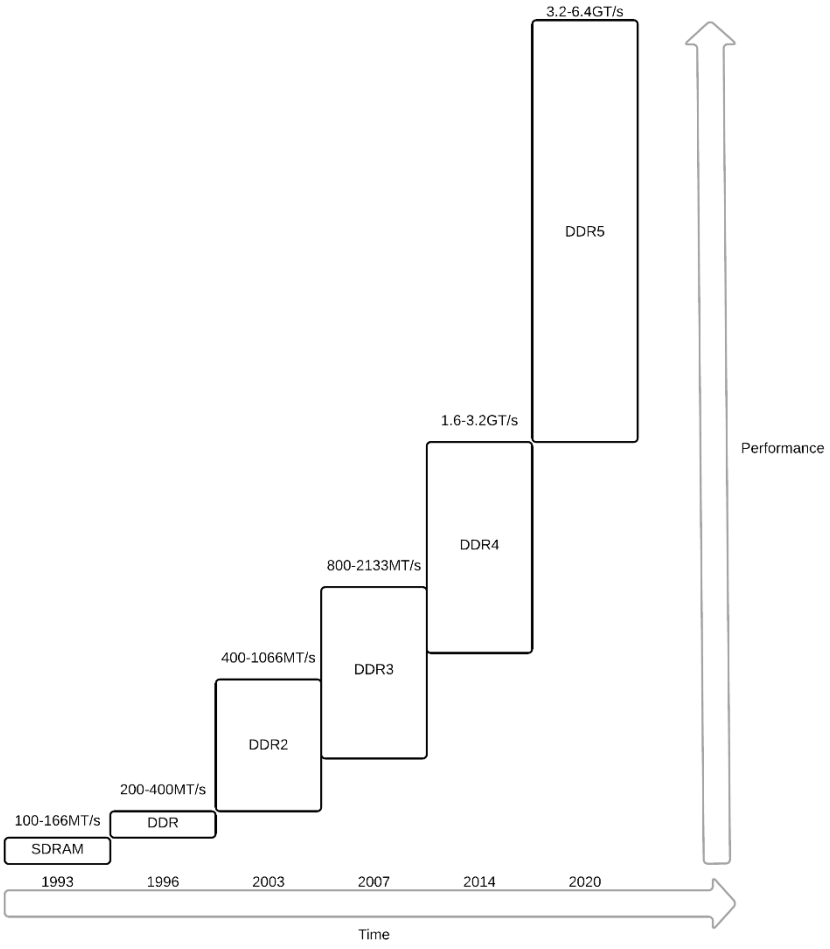

Create and Package New IP
Add Interfaces
Add AXI4 interfaces supported by your peripheral
Enable Interrupt Support
S00_AXI
S_AXI_INTR
pdm_capture_v1.0
Interfaces
S00_AXI
Name
S00_AXI
Interface Type
Lite
Interface Mode
Slave
Data Width (Bits)
32
Memory Size (Bytes)
64
Number of Registers
4
[4..512]
< Back
Next >
Finish
Cancel

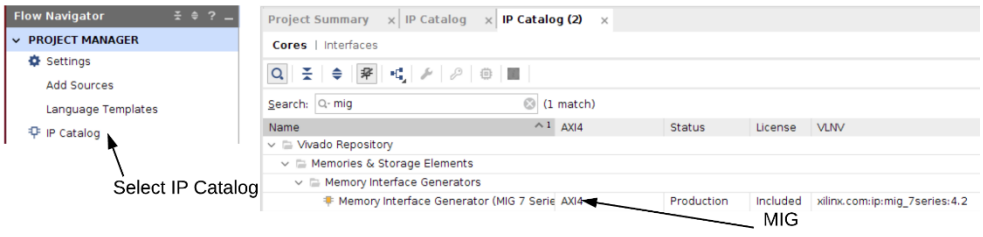

File
Edit
Flow
Tools
Reports
Window
Layout
View
Help
Quick Access
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
BLOCK DESIGN - design_1
Sources
Design
Signals
Board
Design Sources (2)
design_1_wrapper
design_1_i : design_1
adt7420_i2c_bd
adt7420_i2c_mod : adt7
Constraints
Simulation Sources (2)
Utility Sources
Look in:
hdl
adt7420_i2c_bd.v
adt7420_i2c_mod.sv
pdm_inputs.sv
pdm_top.sv
Right click
Add Files
Double click

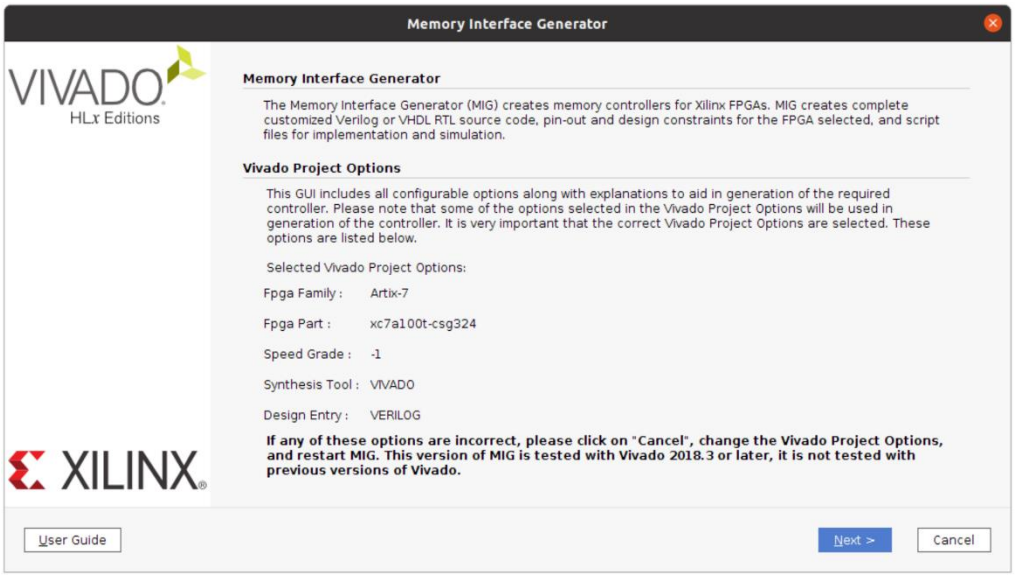

Add Module
Select a module to add to the block design.
Module type:
RTL
Search:
adt7420_i2c_bd (adt7420_i2c_bd.v)
Hide incompatible modules
OK
Cancel

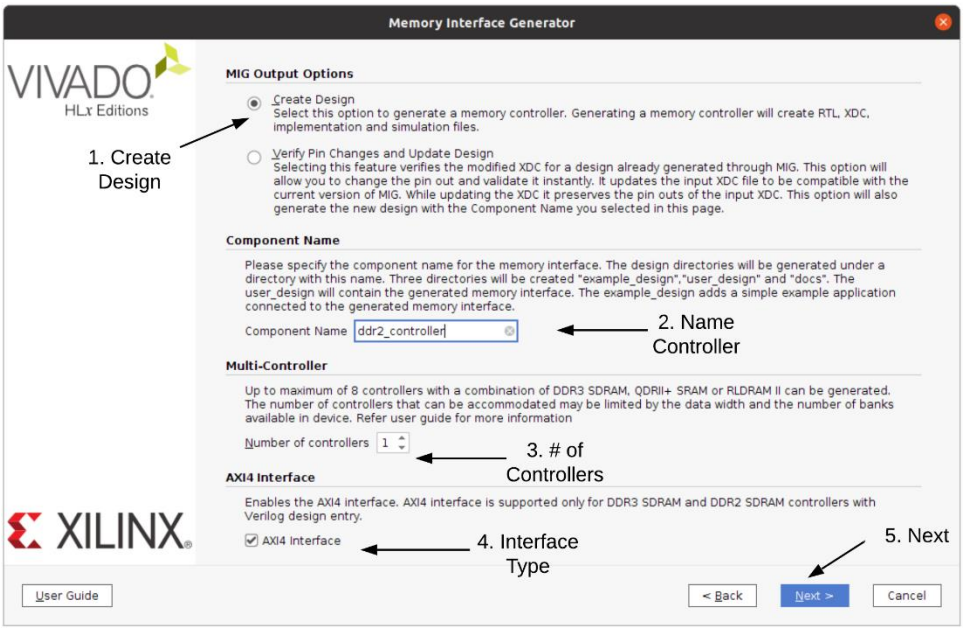

adt7420_i2c_bd_0
clk
RTL
fix_temp
TMP_SCL
TMP_SDA
TMP_INT
TMP_CT
adt7420_i2c_bd_v1_0
adt7420_i2c_0
clk
fix_temp
TMP_SCL
TMP_SDA
TMP_INT
TMP_CT
adt7420_i2c_v1_0

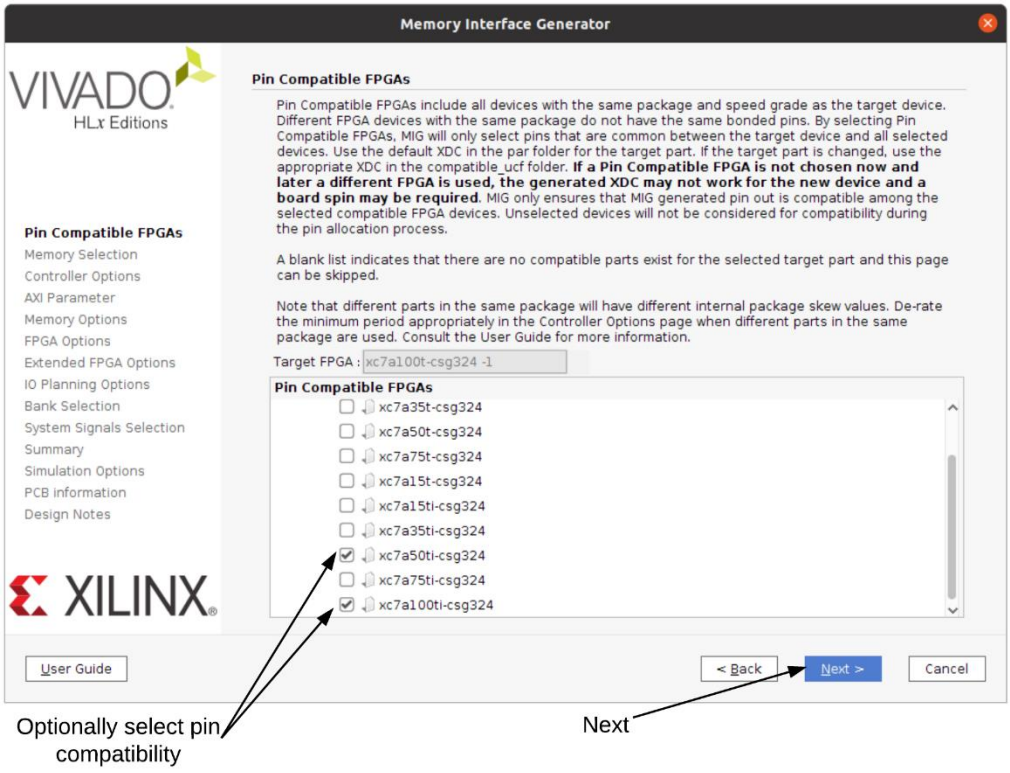
Chapter 8: Lots of Data? MIG and DDR2

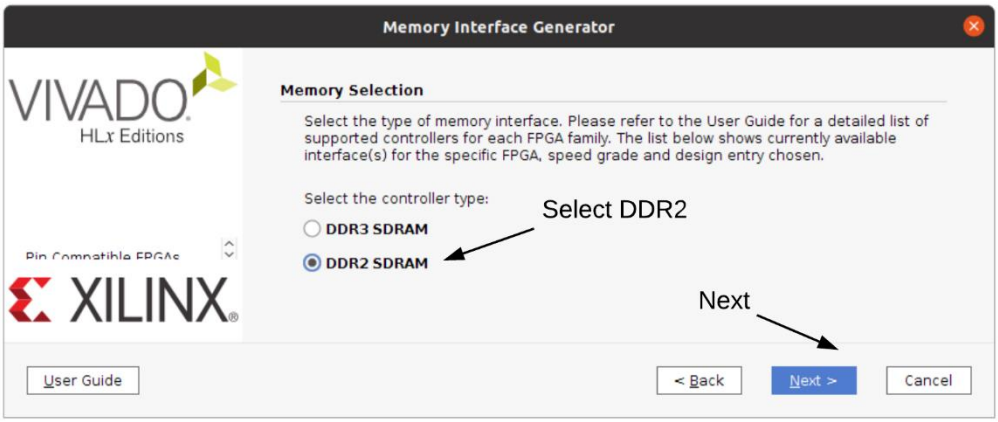


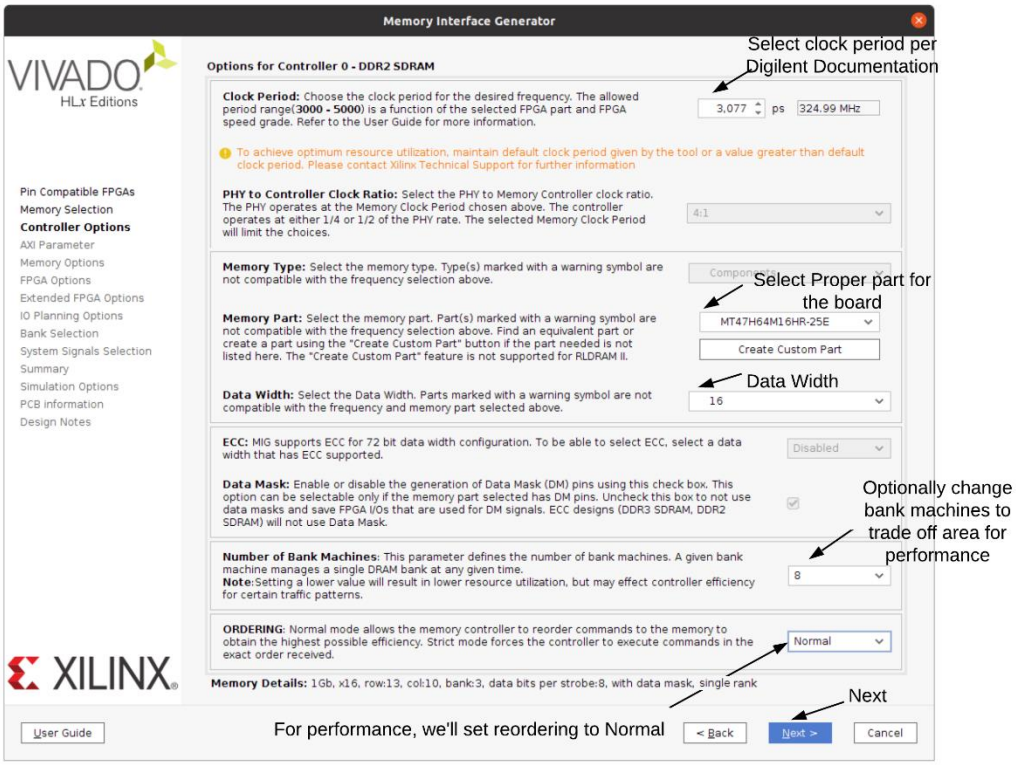


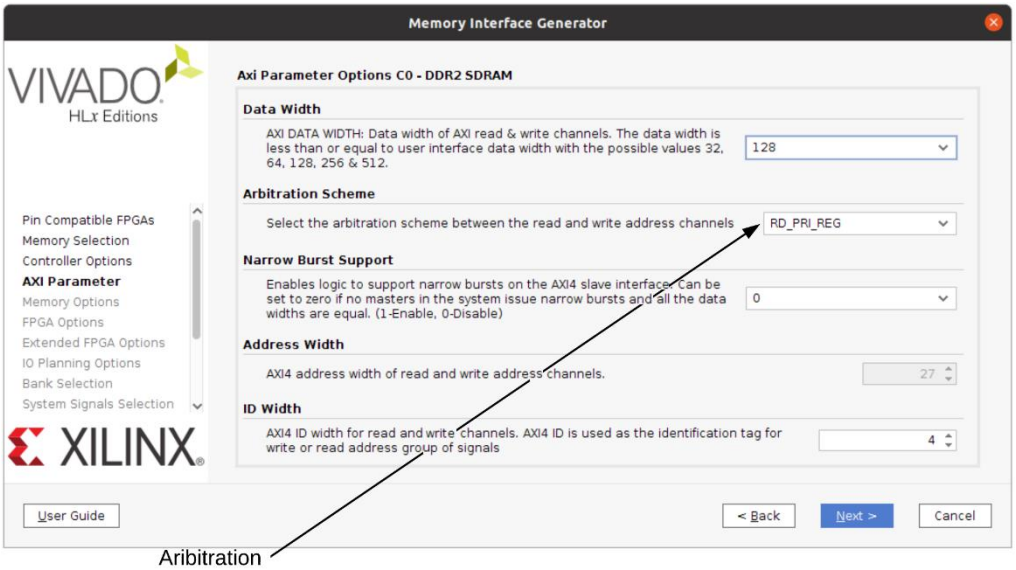

Memory Interface Generator
VIVADO
HLx Editions
Memory Interface Generator
The Memory Interface Generator (MIG) creates memory controllers for Xilinx FPGAs. MIG creates complete customized Verilog or VHDL RTL source code, pin-out and design constraints for the FPGA selected, and script files for implementation and simulation.
Vivado Project Options
This GUI includes all configurable options along with explanations to aid in generation of the required controller. Please note that some of the options selected in the Vivado Project Options will be used in generation of the controller. It is very important that the correct Vivado Project Options are selected. These options are listed below.
Selected Vivado Project Options:
Fpga Family : Artix-7
Fpga Part : xc7a100t-csg324
Speed Grade : -1
Synthesis Tool : VIVADO
Design Entry : VERILOG
If any of these options are incorrect, please click on "Cancel", change the Vivado Project Options, and restart MIG. This version of MIG is tested with Vivado 2018.3 or later, it is not tested with previous versions of Vivado.
XILINX
User Guide
Next >
Cancel

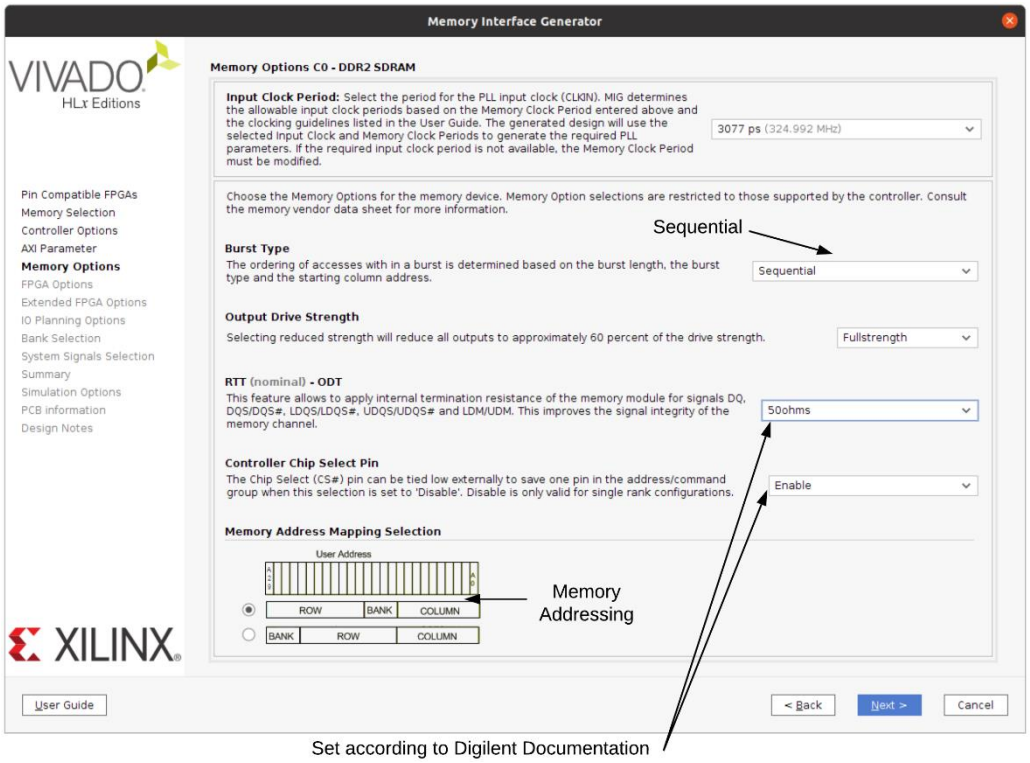

Memory Interface Generator
VIVADO
HLx Editions
MIG Output Options
Create Design
Select this option to generate a memory controller. Generating a memory controller will create RTL, XDC, implementation and simulation files.
Verify Pin Changes and Update Design
Selecting this feature verifies the modified XDC for a design already generated through MIG. This option will allow you to change the pin out and validate it instantly. It updates the input XDC file to be compatible with the current version of MIG. While updating the XDC it preserves the pin outs of the input XDC. This option will also generate the new design with the Component Name you selected in this page.
1. Create Design
Component Name
Please specify the component name for the memory interface. The design directories will be generated under a directory with this name. Three directories will be created "example_design","user_design" and "docs". The user_design will contain the generated memory interface. The example_design adds a simple example application connected to the generated memory interface.
Component Name ddr2_controller
2. Name Controller
Multi-Controller
Up to maximum of 8 controllers with a combination of DDR3 SDRAM, QDRII+ SRAM or RLDRAM II can be generated. The number of controllers that can be accommodated may be limited by the data width and the number of banks available in device. Refer user guide for more information
Number of controllers 1
3. # of Controllers
AXI4 Interface
Enables the AXI4 interface. AXI4 interface is supported only for DDR3 SDRAM and DDR2 SDRAM controllers with Verilog design entry.
AXI4 Interface
4. Interface Type
5. Next
XILINX
User Guide
< Back
Next >
Cancel

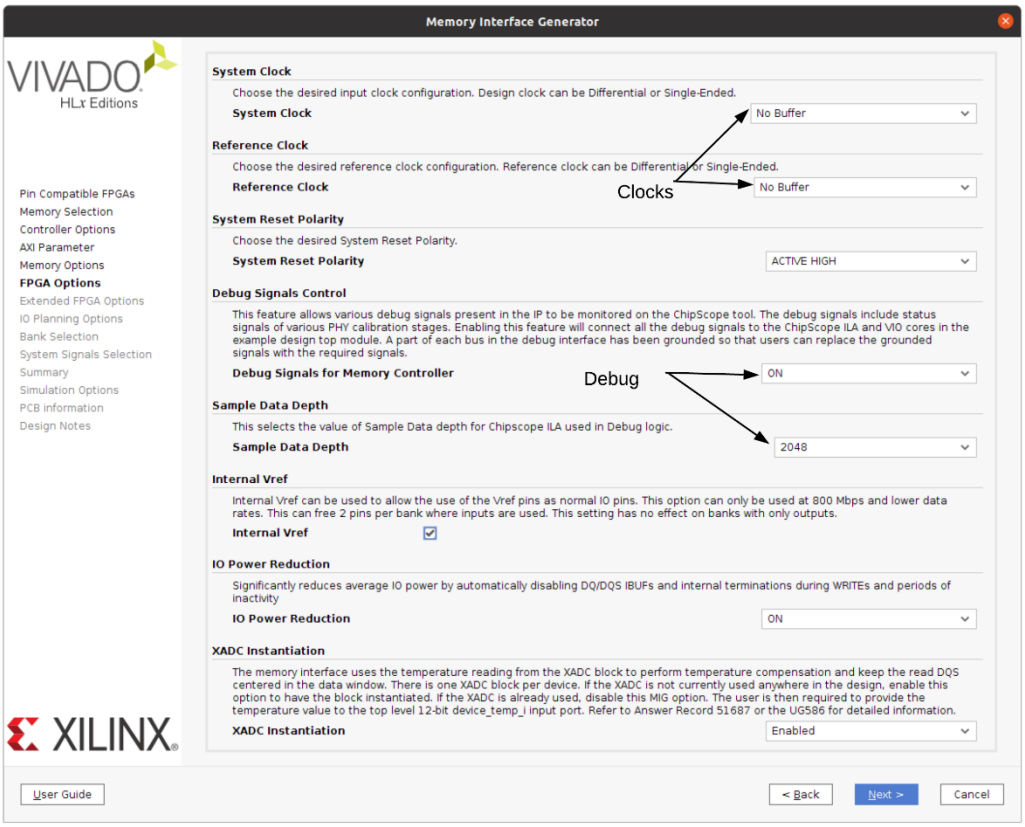

Memory Interface Generator
VIVADO
HLx Editions
Pin Compatible FPGAs
Memory Selection
Controller Options
AXI Parameter
Memory Options
FPGA Options
Extended FPGA Options
IO Planning Options
Bank Selection
System Signals Selection
Summary
Simulation Options
PCB information
Design Notes
XILINX
Pin Compatible FPGAs
Pin Compatible FPGAs include all devices with the same package and speed grade as the target device. Different FPGA devices with the same package do not have the same bonded pins. By selecting Pin Compatible FPGAs, MIG will only select pins that are common between the target device and all selected devices. Use the default XDC in the par folder for the target part. If the target part is changed, use the appropriate XDC in the compatible_ucf folder. If a Pin Compatible FPGA is not chosen now and later a different FPGA is used, the generated XDC may not work for the new device and a board spin may be required. MIG only ensures that MIG generated pin out is compatible among the selected compatible FPGA devices. Unselected devices will not be considered for compatibility during the pin allocation process.
A blank list indicates that there are no compatible parts exist for the selected target part and this page can be skipped.
Note that different parts in the same package will have different internal package skew values. De-rate the minimum period appropriately in the Controller Options page when different parts in the same package are used. Consult the User Guide for more information.
Target FPGA : xc7a100t-csg324 -1
Pin Compatible FPGAs
xc7a35t-csg324
xc7a50t-csg324
xc7a75t-csg324
xc7a15t-csg324
xc7a15ti-csg324
xc7a35ti-csg324
xc7a50ti-csg324
xc7a75ti-csg324
xc7a100ti-csg324
User Guide
< Back
Next >
Cancel
Optionally select pin compatibility
Next

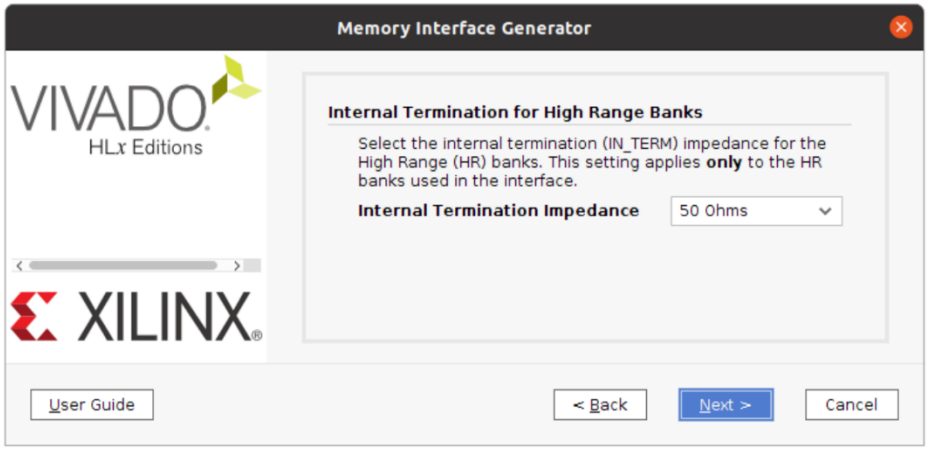

Memory Interface Generator
VIVADO
HLx Editions
XILINX
Memory Selection
Select the type of memory interface. Please refer to the User Guide for a detailed list of supported controllers for each FPGA family. The list below shows currently available interface(s) for the specific FPGA, speed grade and design entry chosen.
Select the controller type:
DDR3 SDRAM
DDR2 SDRAM
Select DDR2
Next
User Guide
< Back
Next >
Cancel

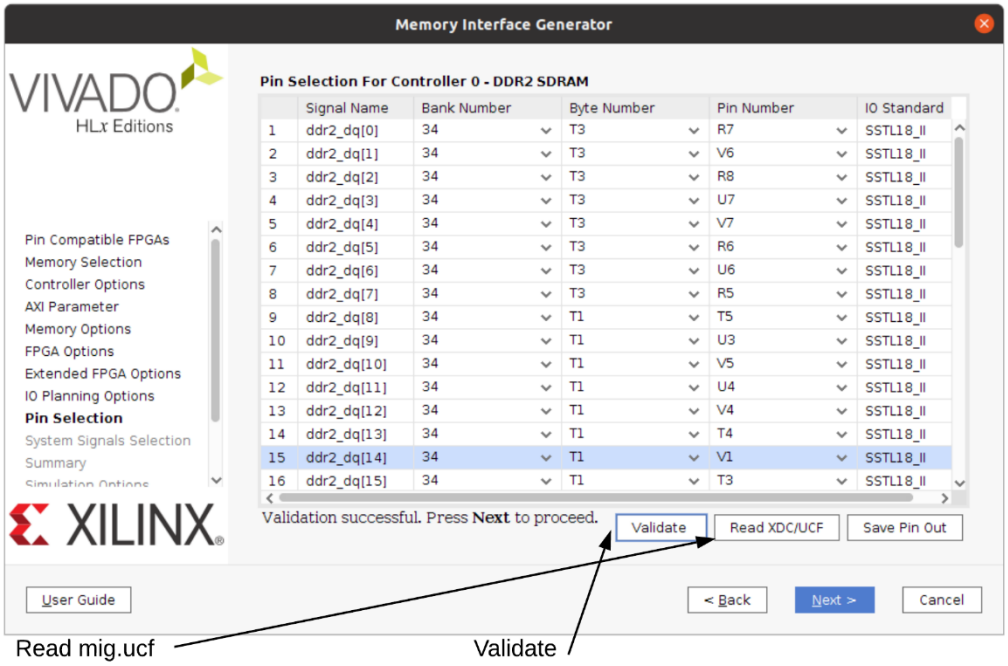

Memory Interface Generator
VIVADO
HLx Editions
Options for Controller 0 - DDR2 SDRAM
Select clock period per Digilent Documentation
Clock Period: Choose the clock period for the desired frequency. The allowed period range(3000 - 5000) is a function of the selected FPGA part and FPGA speed grade. Refer to the User Guide for more information.
3,077
ps
324.99 MHz
To achieve optimum resource utilization, maintain default clock period given by the tool or a value greater than default clock period. Please contact Xilinx Technical Support for further information
PHY to Controller Clock Ratio: Select the PHY to Memory Controller clock ratio. The PHY operates at the Memory Clock Period chosen above. The controller operates at either 1/4 or 1/2 of the PHY rate. The selected Memory Clock Period will limit the choices.
4:1
Memory Type: Select the memory type. Type(s) marked with a warning symbol are not compatible with the frequency selection above.
Select Proper part for the board
Memory Part: Select the memory part. Part(s) marked with a warning symbol are not compatible with the frequency selection above. Find an equivalent part or create a part using the "Create Custom Part" button if the part needed is not listed here. The "Create Custom Part" feature is not supported for RLDRAM II.
MT47H64M16HR-25E
Create Custom Part
Data Width
Data Width: Select the Data Width. Parts marked with a warning symbol are not compatible with the frequency and memory part selected above.
16
ECC: MIG supports ECC for 72 bit data width configuration. To be able to select ECC, select a data width that has ECC supported.
Disabled
Data Mask: Enable or disable the generation of Data Mask (DM) pins using this check box. This option can be selectable only if the memory part selected has DM pins. Uncheck this box to not use data masks and save FPGA I/Os that are used for DM signals. ECC designs (DDR3 SDRAM, DDR2 SDRAM) will not use Data Mask.
Optionally change bank machines to trade off area for performance
Number of Bank Machines: This parameter defines the number of bank machines. A given bank machine manages a single DRAM bank at any given time.
Note:Setting a lower value will result in lower resource utilization, but may effect controller efficiency for certain traffic patterns.
8
ORDERING: Normal mode allows the memory controller to reorder commands to the memory to obtain the highest possible efficiency. Strict mode forces the controller to execute commands in the exact order received.
Normal
Pin Compatible FPGAs
Memory Selection
Controller Options
AXI Parameter
Memory Options
FPGA Options
Extended FPGA Options
IO Planning Options
Bank Selection
System Signals Selection
Summary
Simulation Options
PCB information
Design Notes
XILINX
Memory Details: 1Gb, x16, row:13, col:10, bank:3, data bits per strobe:8, with data mask, single rank
Next
For performance, we'll set reordering to Normal
User Guide
< Back
Next >
Cancel

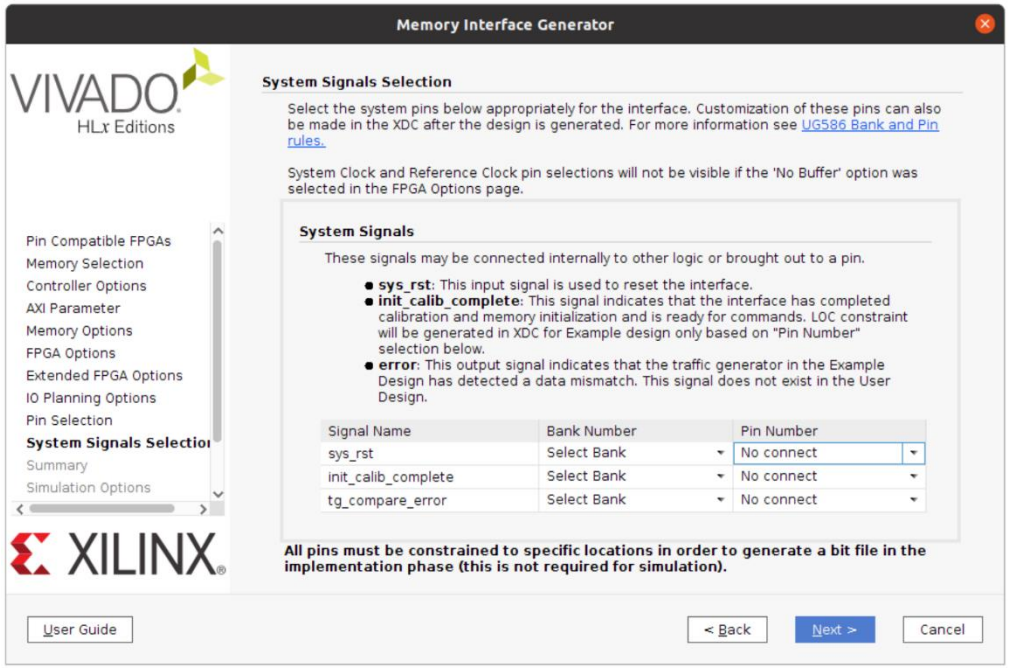

Memory Interface Generator
VIVADO
HLx Editions
Axi Parameter Options C0 - DDR2 SDRAM
Data Width
AXI DATA WIDTH: Data width of AXI read & write channels. The data width is less than or equal to user interface data width with the possible values 32, 64, 128, 256 & 512.
128
Arbitration Scheme
Select the arbitration scheme between the read and write address channels
RD_PRI_REG
Narrow Burst Support
Enables logic to support narrow bursts on the AXI4 slave interface. Can be set to zero if no masters in the system issue narrow bursts and all the data widths are equal. (1-Enable, 0-Disable)
0
Address Width
AXI4 address width of read and write address channels.
27
ID Width
AXI4 ID width for read and write channels. AXI4 ID is used as the identification tag for write or read address group of signals
4
Pin Compatible FPGAs
Memory Selection
Controller Options
AXI Parameter
Memory Options
FPGA Options
Extended FPGA Options
IO Planning Options
Bank Selection
System Signals Selection
XILINX
Aribitration
User Guide
< Back
Next >
Cancel

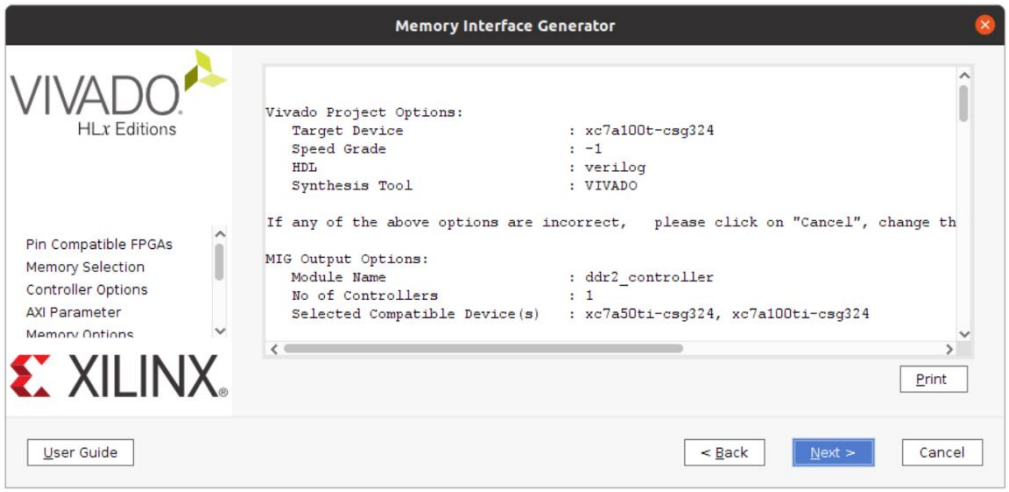

Memory Interface Generator
VIVADO HLx Editions
Memory Options C0 - DDR2 SDRAM
Input Clock Period: Select the period for the PLL input clock (CLKIN). MIG determines the allowable input clock periods based on the Memory Clock Period entered above and the clocking guidelines listed in the User Guide. The generated design will use the selected Input Clock and Memory Clock Periods to generate the required PLL parameters. If the required input clock period is not available, the Memory Clock Period must be modified.
3077 ps (324.992 MHz)
Pin Compatible FPGAs
Memory Selection
Controller Options
AXI Parameter
Memory Options
FPGA Options
Extended FPGA Options
IO Planning Options
Bank Selection
System Signals Selection
Summary
Simulation Options
PCB information
Design Notes
Choose the Memory Options for the memory device. Memory Option selections are restricted to those supported by the controller. Consult the memory vendor data sheet for more information.
Sequential
Burst Type
The ordering of accesses with in a burst is determined based on the burst length, the burst type and the starting column address.
Sequential
Output Drive Strength
Selecting reduced strength will reduce all outputs to approximately 60 percent of the drive strength.
Fullstrength
RTT (nominal) - ODT
This feature allows to apply internal termination resistance of the memory module for signals DQ, DQS/DQS#, LDQS/LDQS#, UDQS/UDQS# and LDM/UDM. This improves the signal integrity of the memory channel.
50ohms
Controller Chip Select Pin
The Chip Select (CS#) pin can be tied low externally to save one pin in the address/command group when this selection is set to 'Disable'. Disable is only valid for single rank configurations.
Enable
Memory Address Mapping Selection
User Address
ROW
BANK
COLUMN
BANK
ROW
COLUMN
Memory Addressing
XILINX
User Guide
< Back
Next >
Cancel
Set according to Digilent Documentation

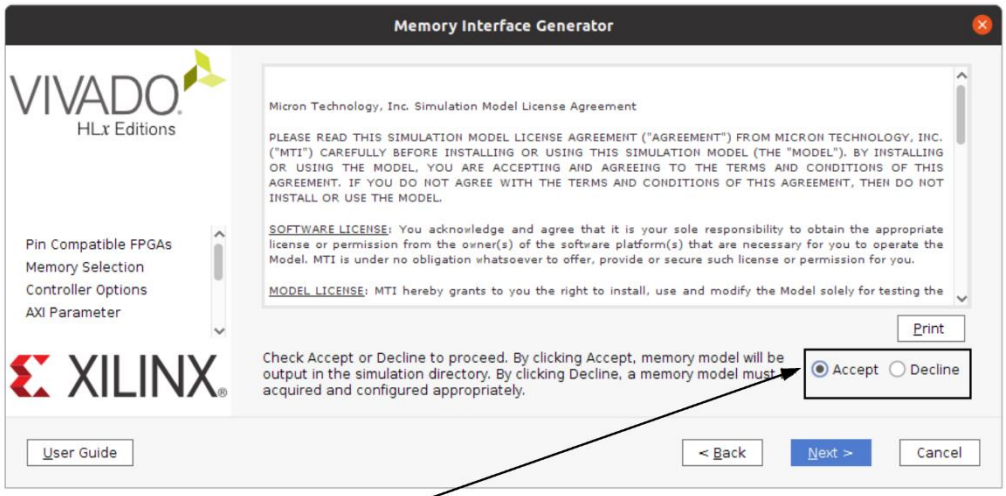

Memory Interface Generator
VIVADO HLx Editions
System Clock
Choose the desired input clock configuration. Design clock can be Differential or Single-Ended.
System Clock
No Buffer
Reference Clock
Choose the desired reference clock configuration. Reference clock can be Differential or Single-Ended.
Reference Clock
No Buffer
Clocks
System Reset Polarity
Choose the desired System Reset Polarity.
System Reset Polarity
ACTIVE HIGH
Debug Signals Control
This feature allows various debug signals present in the IP to be monitored on the ChipScope tool. The debug signals include status signals of various PHY calibration stages. Enabling this feature will connect all the debug signals to the ChipScope ILA and VIO cores in the example design top module. A part of each bus in the debug interface has been grounded so that users can replace the grounded signals with the required signals.
Debug Signals for Memory Controller
ON
Debug
Sample Data Depth
This selects the value of Sample Data depth for Chipscope ILA used in Debug logic.
Sample Data Depth
2048
Internal Vref
Internal Vref can be used to allow the use of the Vref pins as normal IO pins. This option can only be used at 800 Mbps and lower data rates. This can free 2 pins per bank where inputs are used. This setting has no effect on banks with only outputs.
Internal Vref
IO Power Reduction
Significantly reduces average IO power by automatically disabling DQ/DQS IBUFs and internal terminations during WRITEs and periods of inactivity
IO Power Reduction
ON
XADC Instantiation
The memory interface uses the temperature reading from the XADC block to perform temperature compensation and keep the read DQS centered in the data window. There is one XADC block per device. If the XADC is not currently used anywhere in the design, enable this option to have the block instantiated. If the XADC is already used, disable this MIG option. The user is then required to provide the temperature value to the top level 12-bit device_temp_i input port. Refer to Answer Record 51687 or the UG586 for detailed information.
XADC Instantiation
Enabled
Pin Compatible FPGAs
Memory Selection
Controller Options
AXI Parameter
Memory Options
FPGA Options
Extended FPGA Options
IO Planning Options
Bank Selection
System Signals Selection
Summary
Simulation Options
PCB information
Design Notes
XILINX
User Guide
< Back
Next >
Cancel


Memory Interface Generator
VIVADO
HLx Editions
XILINX
Internal Termination for High Range Banks
Select the internal termination (IN_TERM) impedance for the High Range (HR) banks. This setting applies only to the HR banks used in the interface.
Internal Termination Impedance
50 Ohms
User Guide
< Back
Next >
Cancel

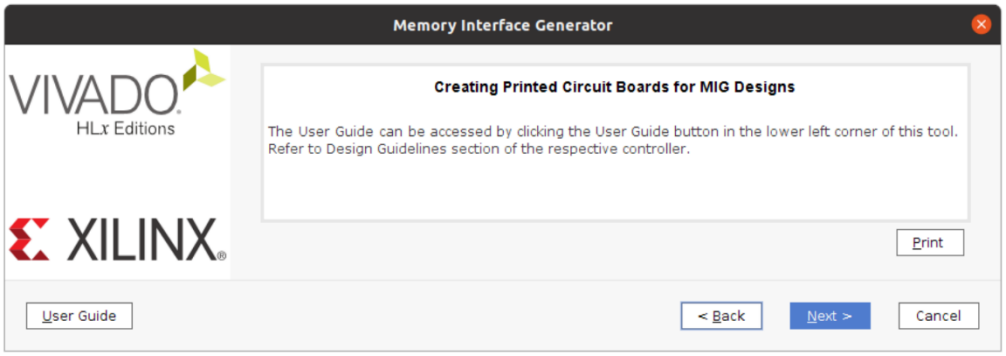

Memory Interface Generator
VIVADO
HLx Editions
XILINX
Pin Compatible FPGAs
Memory Selection
Controller Options
AXI Parameter
Memory Options
FPGA Options
Extended FPGA Options
IO Planning Options
Pin Selection
System Signals Selection
Summary
Pin Selection For Controller 0 - DDR2 SDRAM
Signal Name | Bank Number | Byte Number | Pin Number | IO Standard
1 ddr2_dq[0] 34 T3 R7 SSTL18_II
2 ddr2_dq[1] 34 T3 V6 SSTL18_II
3 ddr2_dq[2] 34 T3 R8 SSTL18_II
4 ddr2_dq[3] 34 T3 U7 SSTL18_II
5 ddr2_dq[4] 34 T3 V7 SSTL18_II
6 ddr2_dq[5] 34 T3 R6 SSTL18_II
7 ddr2_dq[6] 34 T3 U6 SSTL18_II
8 ddr2_dq[7] 34 T3 R5 SSTL18_II
9 ddr2_dq[8] 34 T1 T5 SSTL18_II
10 ddr2_dq[9] 34 T1 U3 SSTL18_II
11 ddr2_dq[10] 34 T1 V5 SSTL18_II
12 ddr2_dq[11] 34 T1 U4 SSTL18_II
13 ddr2_dq[12] 34 T1 V4 SSTL18_II
14 ddr2_dq[13] 34 T1 T4 SSTL18_II
15 ddr2_dq[14] 34 T1 V1 SSTL18_II
16 ddr2_dq[15] 34 T1 T3 SSTL18_II
Validation successful. Press Next to proceed.
Validate
Read XDC/UCF
Save Pin Out
User Guide
< Back
Next >
Cancel
Read mig.ucf
Validate

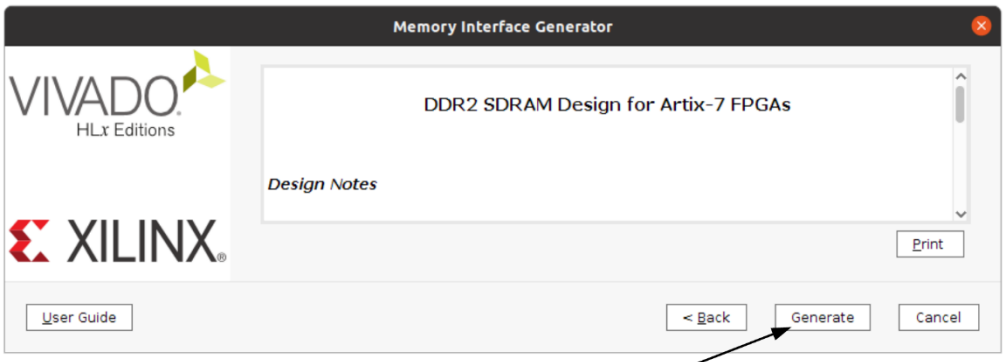

Memory Interface Generator
VIVADO
HLx Editions
Pin Compatible FPGAs
Memory Selection
Controller Options
AXI Parameter
Memory Options
FPGA Options
Extended FPGA Options
IO Planning Options
Pin Selection
System Signals Selectio
Summary
Simulation Options
XILINX
System Signals Selection
Select the system pins below appropriately for the interface. Customization of these pins can also be made in the XDC after the design is generated. For more information see UG586 Bank and Pin rules.
System Clock and Reference Clock pin selections will not be visible if the 'No Buffer' option was selected in the FPGA Options page.
System Signals
These signals may be connected internally to other logic or brought out to a pin.
sys_rst: This input signal is used to reset the interface.
init_calib_complete: This signal indicates that the interface has completed calibration and memory initialization and is ready for commands. LOC constraint will be generated in XDC for Example design only based on "Pin Number" selection below.
error: This output signal indicates that the traffic generator in the Example Design has detected a data mismatch. This signal does not exist in the User Design.
Signal Name
Bank Number
Pin Number
sys_rst
Select Bank
No connect
init_calib_complete
Select Bank
No connect
tg_compare_error
Select Bank
No connect
All pins must be constrained to specific locations in order to generate a bit file in the implementation phase (this is not required for simulation).
User Guide
< Back
Next >
Cancel


Memory Interface Generator
VIVADO
HLx Editions
Pin Compatible FPGAs
Memory Selection
Controller Options
AXI Parameter
Memory Options
XILINX
Vivado Project Options:
Target Device : xc7a100t-csg324
Speed Grade : -1
HDL : verilog
Synthesis Tool : VIVADO
If any of the above options are incorrect, please click on "Cancel", change th
MIG Output Options:
Module Name : ddr2_controller
No of Controllers : 1
Selected Compatible Device(s) : xc7a50ti-csg324, xc7a100ti-csg324
Print
User Guide
< Back
Next >
Cancel



Accept for memory model

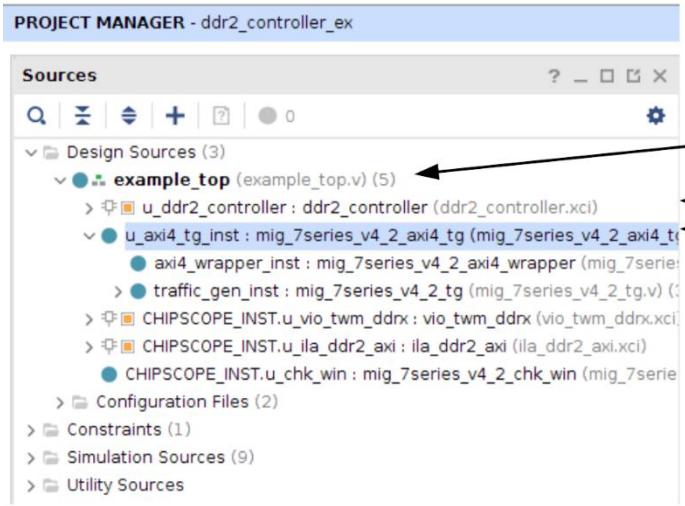




Generate Memory Controller

Right click and select "Open IP Example Design"

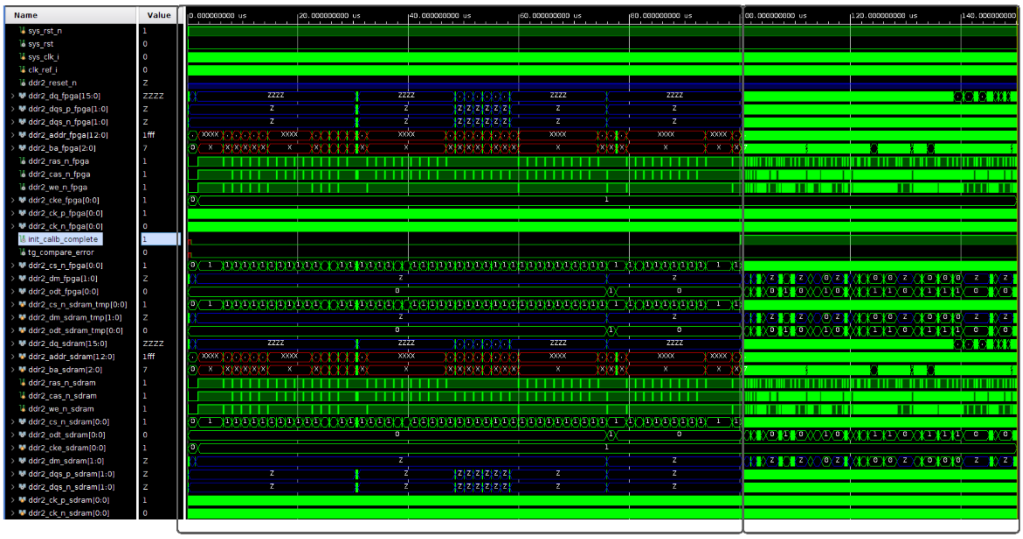
Select directory



Example top level

Our DDR2 Controller

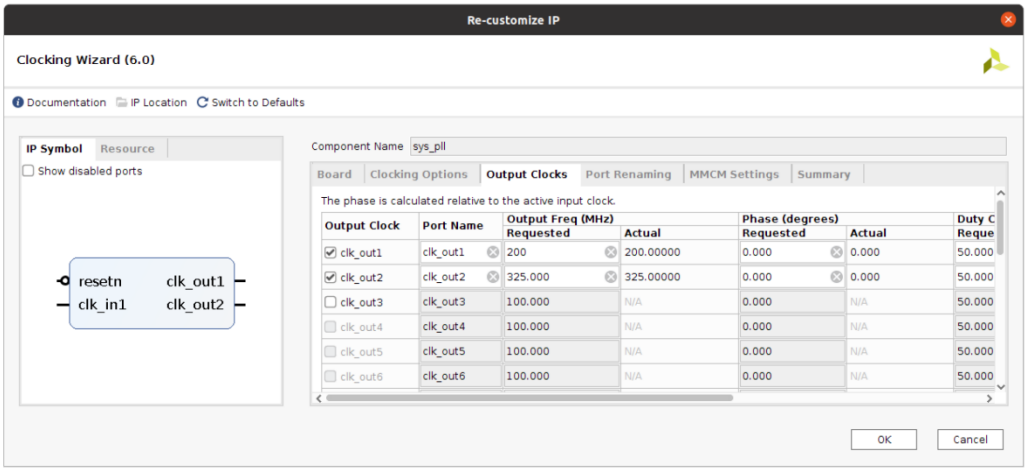
Xilinx Traffic Generator

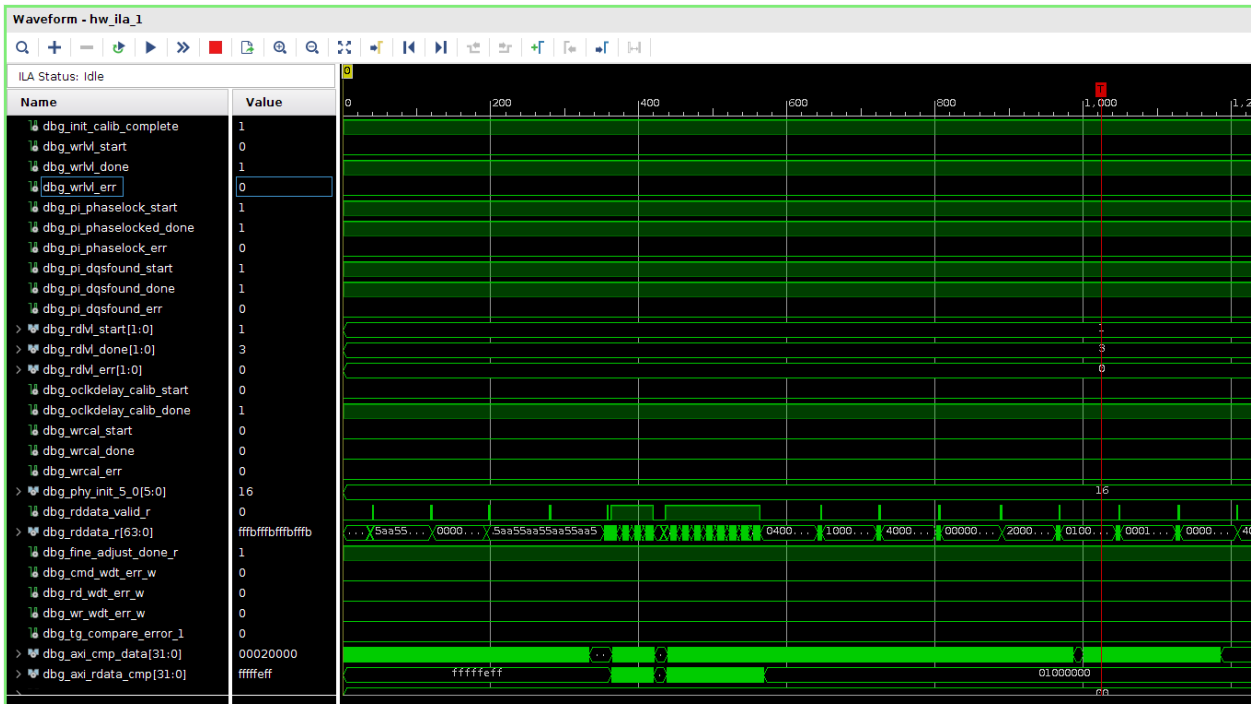


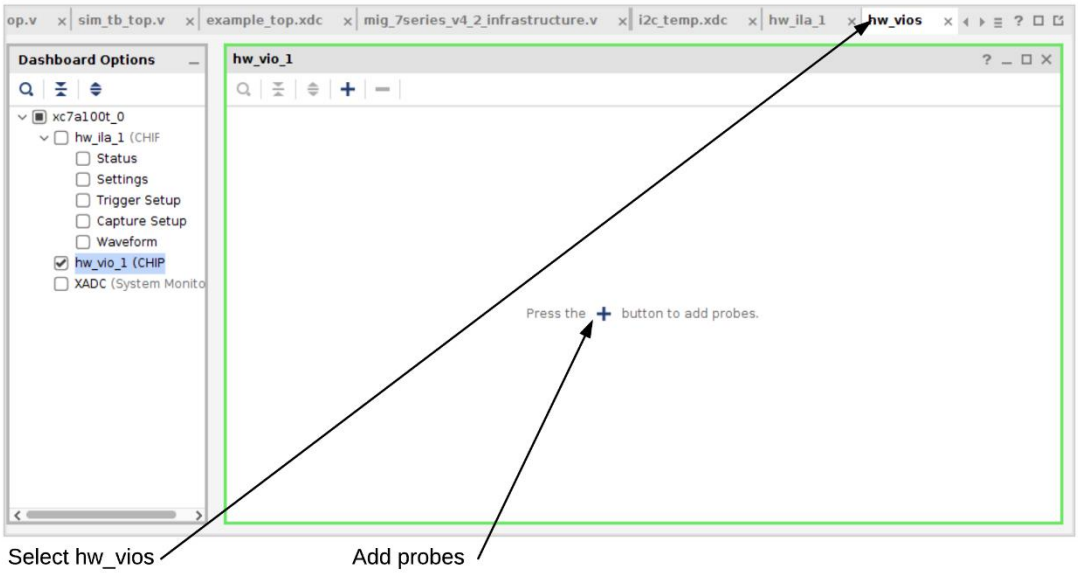
Device Initialization and Calibration

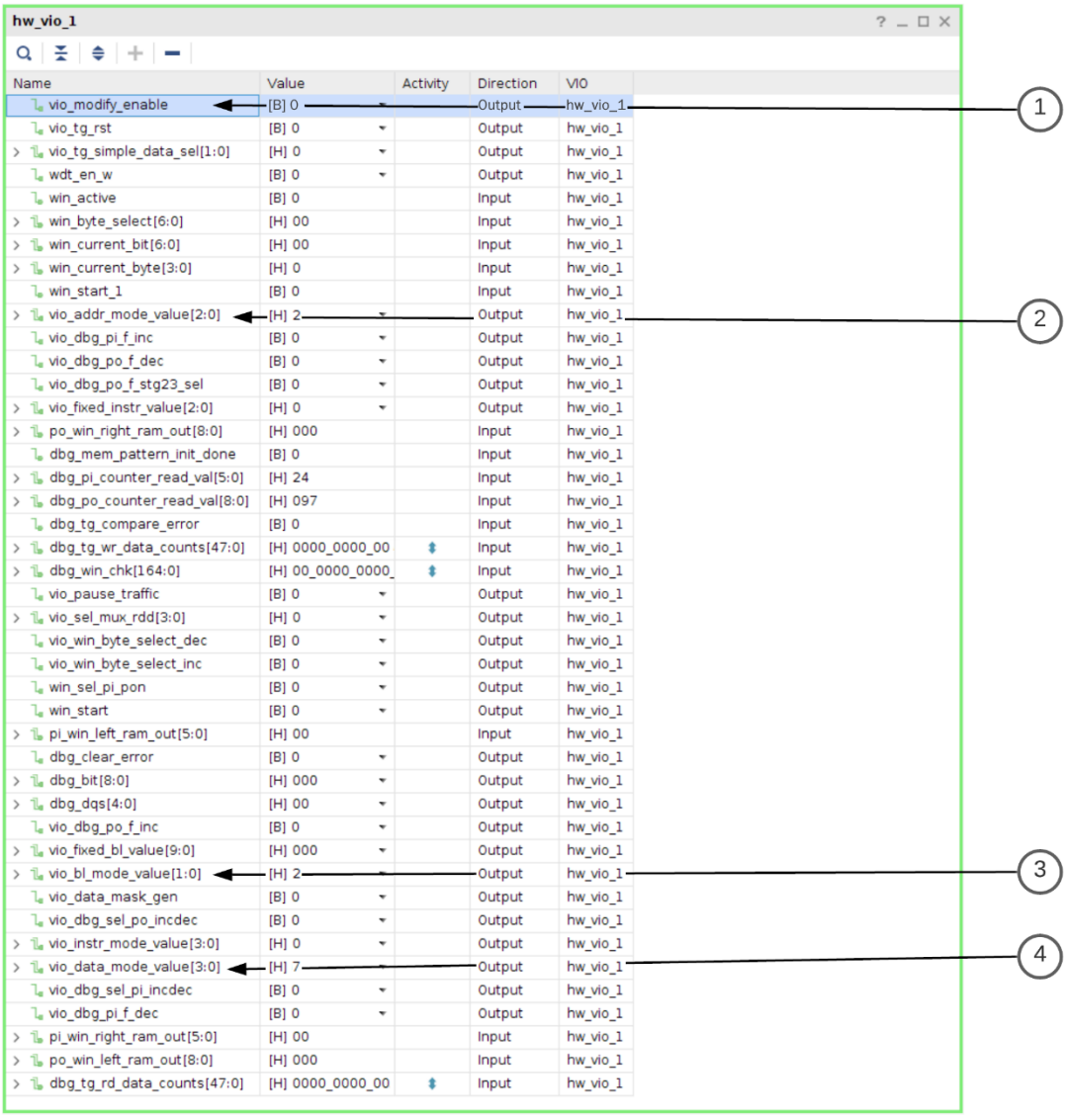
Traffic Generator Test

```
548  //*****************************************************************************
549  // Reporting the test case status
550  // Status reporting logic exists both in simulation test bench (sim_tb_top)
551  // and sim.do file for ModelSim. Any update in simulation run time or time out
552  // in this file need to be updated in sim.do file as well.
553  //*****************************************************************************
554  initial
555  begin : Logging
556     fork
557        begin : calibration_done
558           wait (init_calib_complete);
559           $display("Calibration Done");
560           #50000000.0;
561           if (!tg_compare_error) begin
562              $display("TEST PASSED");
563           end
564           else begin
565              $display("TEST FAILED: DATA ERROR");
566           end
567           disable calib_not_done;
568            $finish;
569        end
```

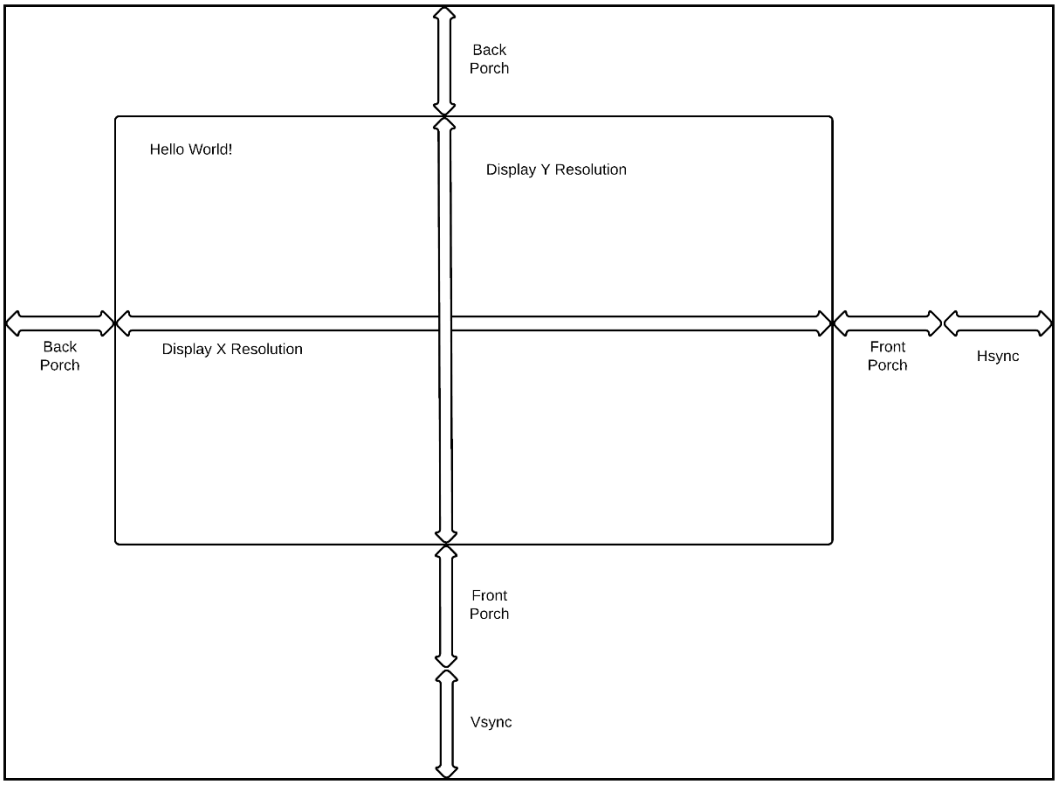


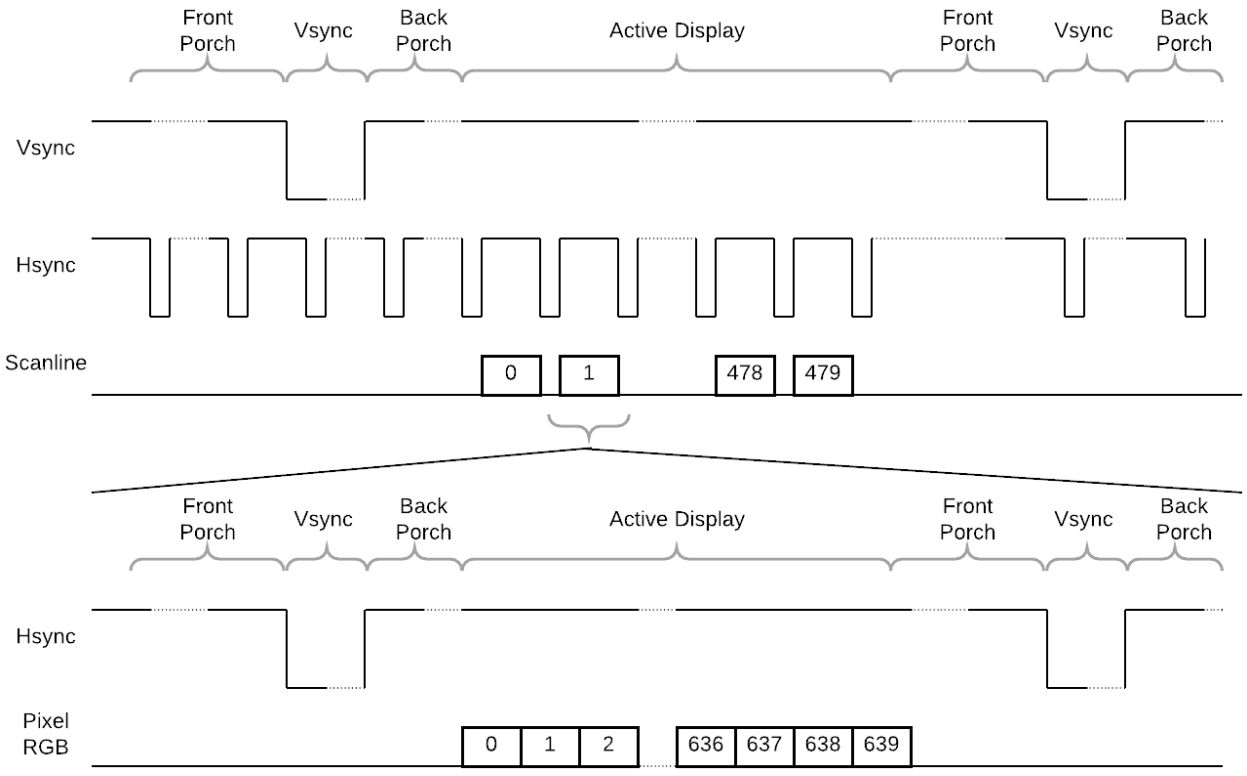

Waveform - hw_ila_1
ILA Status: Idle
Name
Value
dbg_init_calib_complete
dbg_wrlvl_start
dbg_wrlvl_done
dbg_wrlvl_err
dbg_pi_phaselock_start
dbg_pi_phaselocked_done
dbg_pi_phaselock_err
dbg_pi_dqsfound_start
dbg_pi_dqsfound_done
dbg_pi_dqsfound_err
dbg_rdlvl_start[1:0]
dbg_rdlvl_done[1:0]
dbg_rdlvl_err[1:0]
dbg_oclkdelay_calib_start
dbg_oclkdelay_calib_done
dbg_wrcal_start
dbg_wrcal_done
dbg_wrcal_err
dbg_phy_init_5_0[5:0]
dbg_rddata_valid_r
dbg_rddata_r[63:0]
dbg_fine_adjust_done_r
dbg_cmd_wdt_err_w
dbg_rd_wdt_err_w
dbg_wr_wdt_err_w
dbg_tg_compare_error_1
dbg_axi_cmp_data[31:0]
dbg_axi_rdata_cmp[31:0]
00020000
ffffffff
01000000

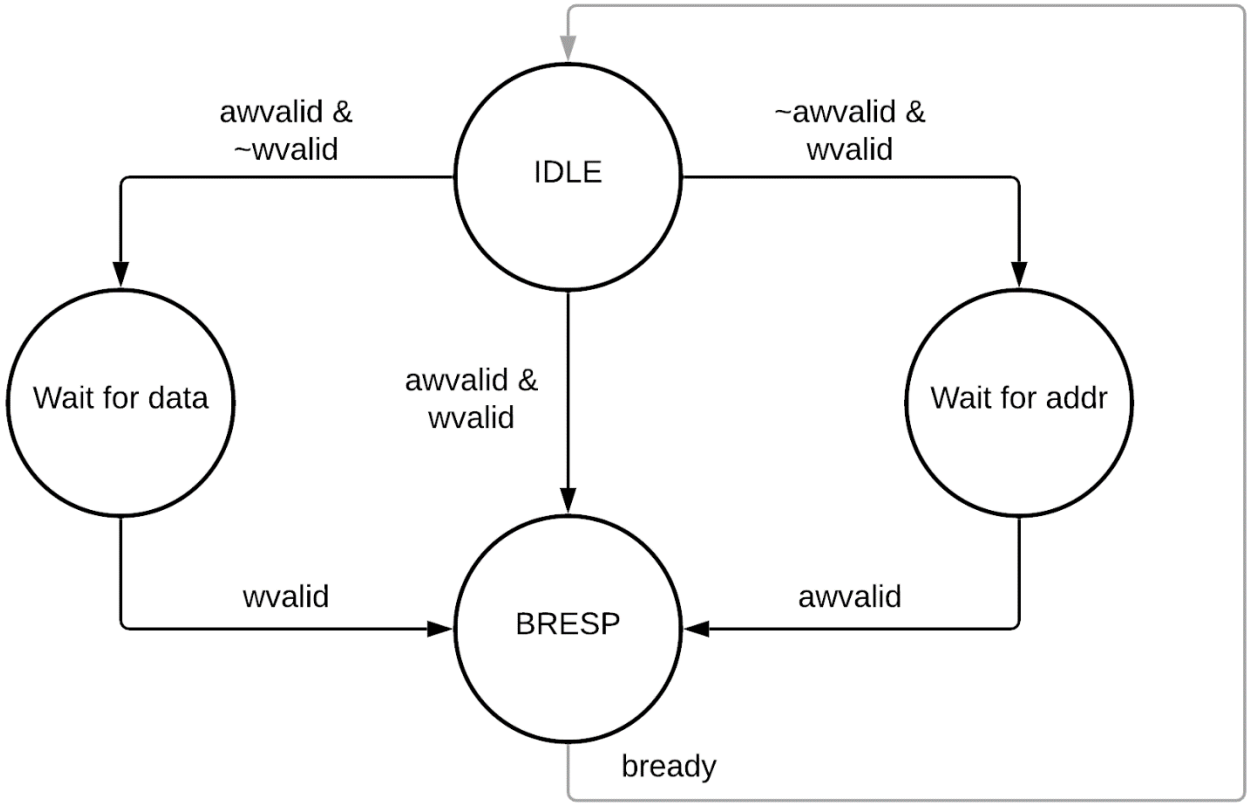

op.v
sim_tb_top.v
example_top.xdc
mig_7series_v4_2_infrastructure.v
i2c_temp.xdc
hw_ila_1
hw_vios
Dashboard Options
xc7a100t_0
hw_ila_1 (CHIF
Status
Settings
Trigger Setup
Capture Setup
Waveform
hw_vio_1 (CHIP
XADC (System Monito
hw_vio_1
Press the + button to add probes.
Select hw_vios
Add probes

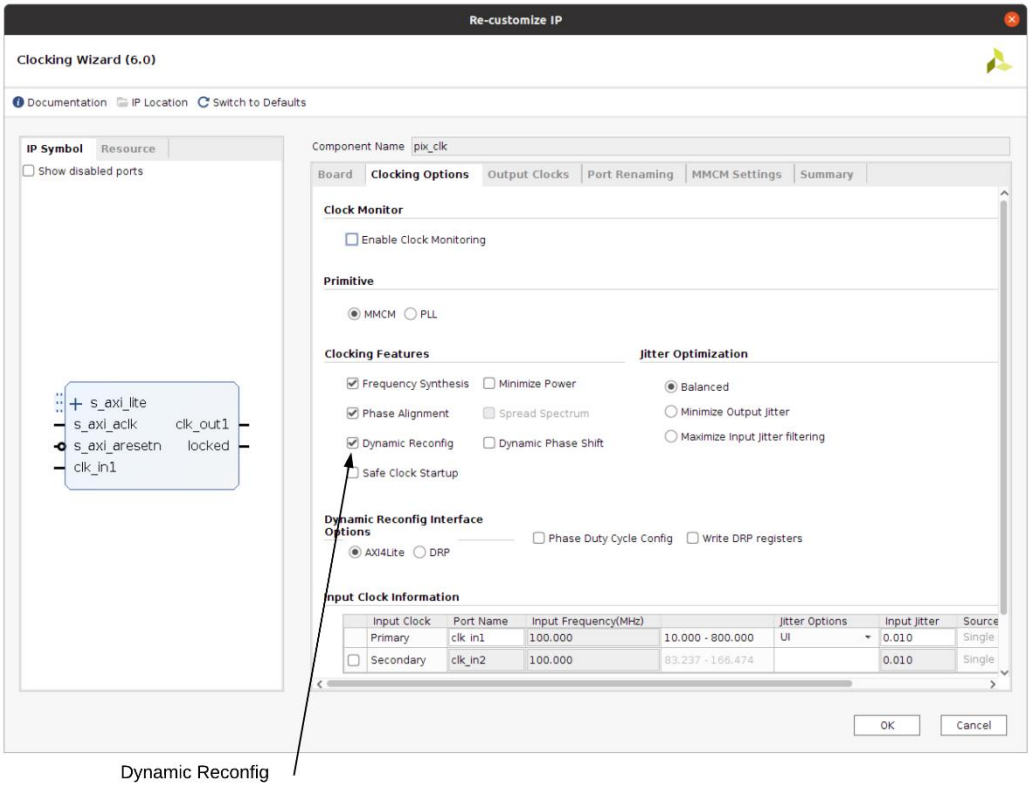

hw_vio_1
Name
Value
Activity
Direction
VIO
vio_modify_enable
[B] 0
Output
hw_vio_1
vio_tg_rst
[B] 0
Output
hw_vio_1
vio_tg_simple_data_sel[1:0]
[H] 0
Output
hw_vio_1
wdt_en_w
[B] 0
Output
hw_vio_1
win_active
[B] 0
Input
hw_vio_1
win_byte_select[6:0]
[H] 00
Input
hw_vio_1
win_current_bit[6:0]
[H] 00
Input
hw_vio_1
win_current_byte[3:0]
[H] 0
Input
hw_vio_1
win_start_1
[B] 0
Input
hw_vio_1
vio_addr_mode_value[2:0]
[H] 2
Output
hw_vio_1
vio_dbg_pi_f_inc
[B] 0
Output
hw_vio_1
vio_dbg_po_f_dec
[B] 0
Output
hw_vio_1
vio_dbg_po_f_stg23_sel
[B] 0
Output
hw_vio_1
vio_fixed_instr_value[2:0]
[H] 0
Output
hw_vio_1
po_win_right_ram_out[8:0]
[H] 000
Input
hw_vio_1
dbg_mem_pattern_init_done
[B] 0
Input
hw_vio_1
dbg_pi_counter_read_val[5:0]
[H] 24
Input
hw_vio_1
dbg_po_counter_read_val[8:0]
[H] 097
Input
hw_vio_1
dbg_tg_compare_error
[B] 0
Input
hw_vio_1
dbg_tg_wr_data_counts[47:0]
[H] 0000_0000_00
Input
hw_vio_1
dbg_win_chk[164:0]
[H] 00_0000_0000_
Input
hw_vio_1
vio_pause_traffic
[B] 0
Output
hw_vio_1
vio_sel_mux_rdd[3:0]
[H] 0
Output
hw_vio_1
vio_win_byte_select_dec
[B] 0
Output
hw_vio_1
vio_win_byte_select_inc
[B] 0
Output
hw_vio_1
win_sel_pi_pon
[B] 0
Output
hw_vio_1
win_start
[B] 0
Output
hw_vio_1
pi_win_left_ram_out[5:0]
[H] 00
Input
hw_vio_1
dbg_clear_error
[B] 0
Output
hw_vio_1
dbg_bit[8:0]
[H] 000
Output
hw_vio_1
dbg_dqs[4:0]
[H] 00
Output
hw_vio_1
vio_dbg_po_f_inc
[B] 0
Output
hw_vio_1
vio_fixed_bl_value[9:0]
[H] 000
Output
hw_vio_1
vio_bl_mode_value[1:0]
[H] 2
Output
hw_vio_1
vio_data_mask_gen
[B] 0
Output
hw_vio_1
vio_dbg_sel_po_incdec
[B] 0
Output
hw_vio_1
vio_instr_mode_value[3:0]
[H] 0
Output
hw_vio_1
vio_data_mode_value[3:0]
[H] 7
Output
hw_vio_1
vio_dbg_sel_pi_incdec
[B] 0
Output
hw_vio_1
vio_dbg_pi_f_dec
[B] 0
Output
hw_vio_1
pi_win_right_ram_out[5:0]
[H] 00
Input
hw_vio_1
po_win_left_ram_out[8:0]
[H] 000
Input
hw_vio_1
dbg_tg_rd_data_counts[47:0]
[H] 0000_0000_00
Input
hw_vio_1
1
2
3
4

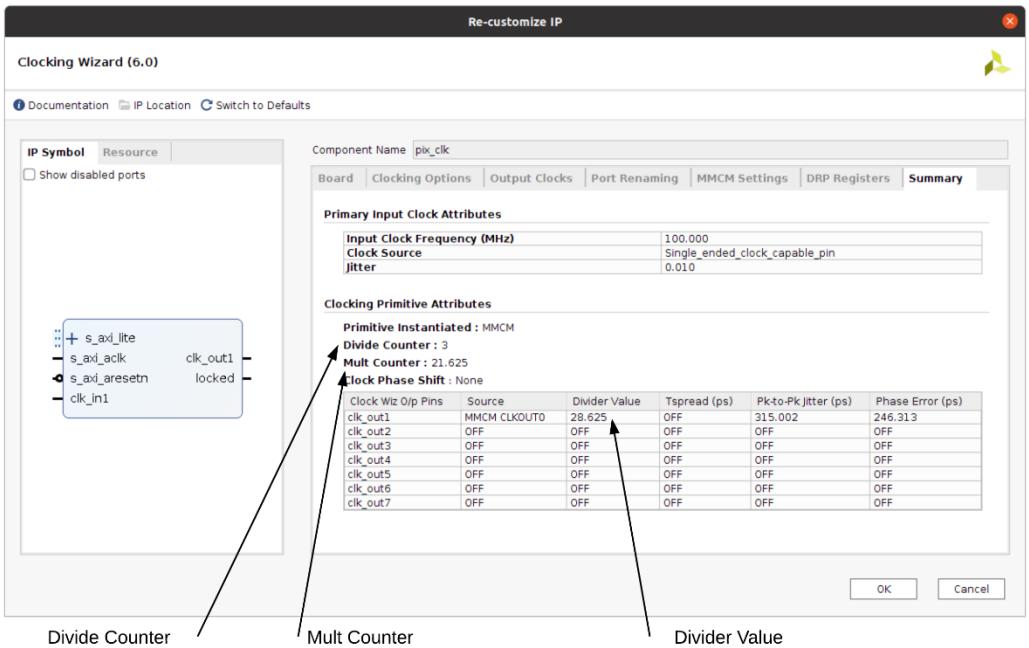
Chapter 9: A Better Way to Display – VGA

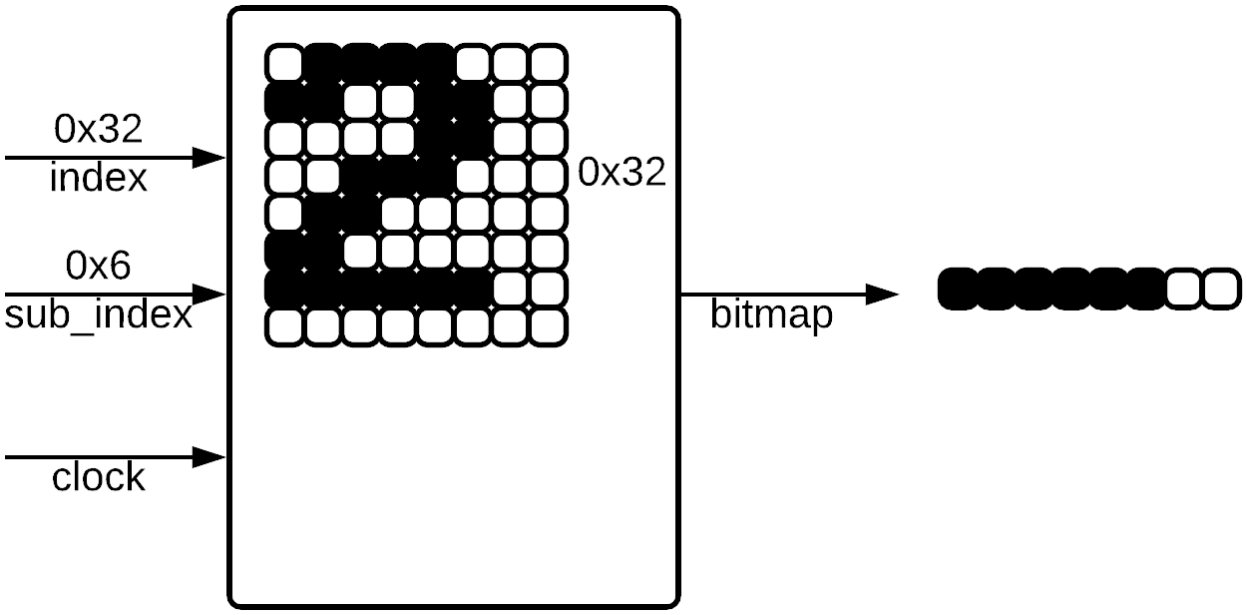


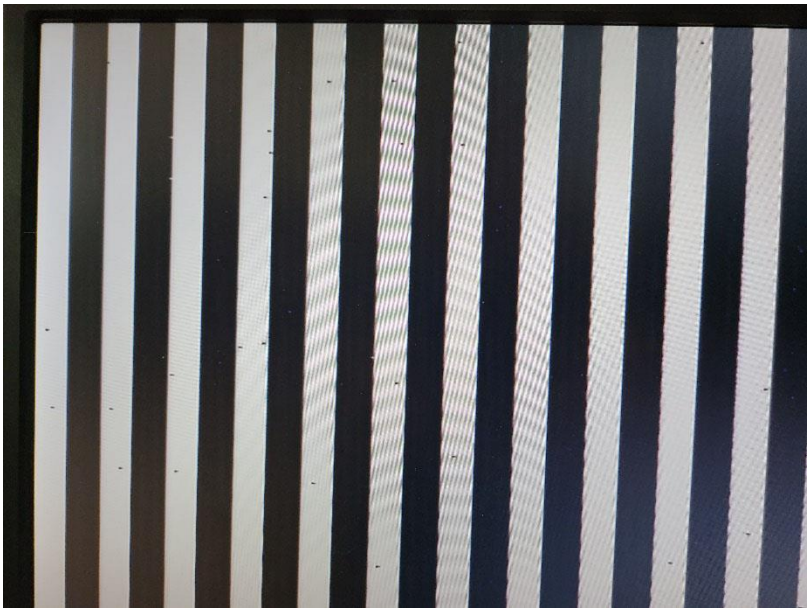


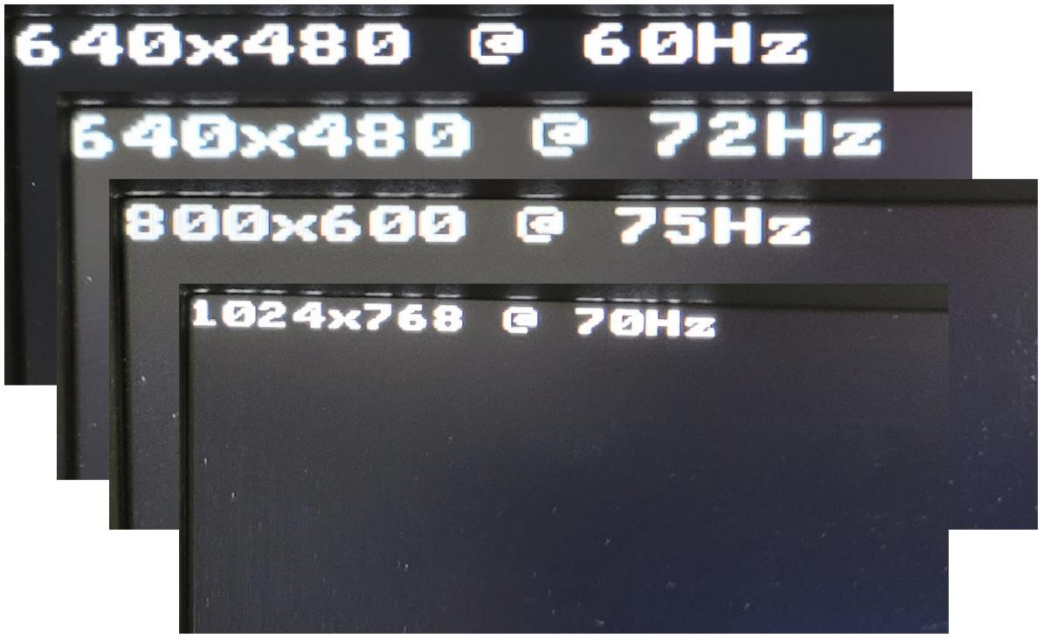

awvalid &
~wvalid
IDLE
~awvalid &
wvalid
Wait for data
awvalid &
wvalid
Wait for addr
wvalid
BRESP
awvalid
bready


Re-customize IP
Clocking Wizard (6.0)
Documentation
IP Location
Switch to Defaults
IP Symbol
Resource
Show disabled ports
s_axi_lite
s_axi_aclk
s_axi_aresetn
clk_in1
clk_out1
locked
Component Name
pix_clk
Board
Clocking Options
Output Clocks
Port Renaming
MMCM Settings
Summary
Clock Monitor
Enable Clock Monitoring
Primitive
MMCM
PLL
Clocking Features
Frequency Synthesis
Minimize Power
Phase Alignment
Spread Spectrum
Dynamic Reconfig
Dynamic Phase Shift
Safe Clock Startup
Jitter Optimization
Balanced
Minimize Output Jitter
Maximize Input Jitter filtering
Dynamic Reconfig Interface Options
AXI4Lite
DRP
Phase Duty Cycle Config
Write DRP registers
Input Clock Information
Input Clock
Port Name
Input Frequency(MHz)
Jitter Options
Input Jitter
Source
Primary
clk_in1
100.000
10.000 - 800.000
UI
0.010
Single
Secondary
clk_in2
100.000
83.237 - 166.474
0.010
Single
OK
Cancel
Dynamic Reconfig

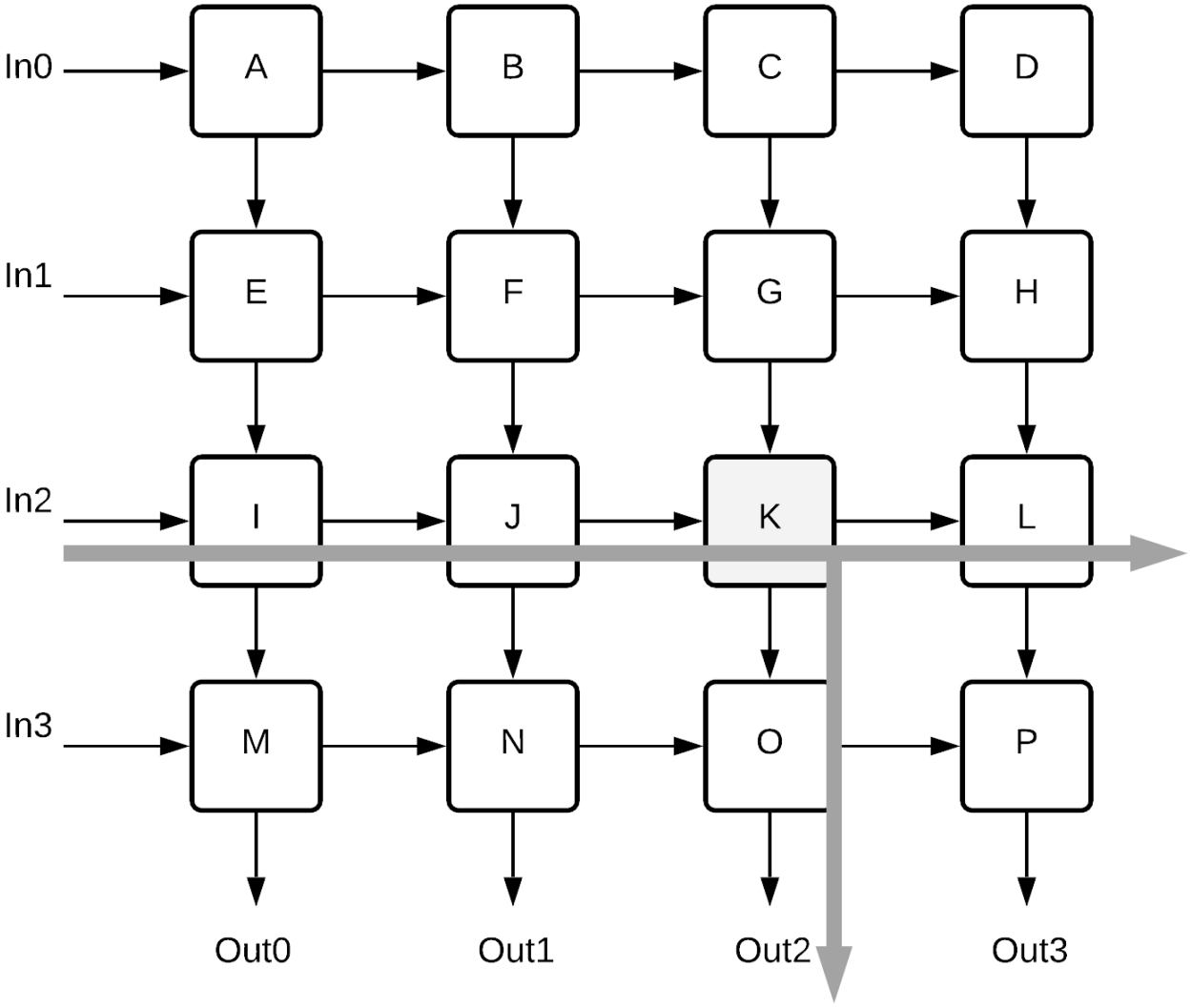

Re-customize IP
Clocking Wizard (6.0)
Documentation
IP Location
Switch to Defaults
IP Symbol
Resource
Show disabled ports
s_axi_lite
s_axi_aclk
s_axi_aresetn
clk_in1
clk_out1
locked
Component Name
pix_clk
Board
Clocking Options
Output Clocks
Port Renaming
MMCM Settings
DRP Registers
Summary
Primary Input Clock Attributes
Input Clock Frequency (MHz) 100.000
Clock Source Single_ended_clock_capable_pin
Jitter 0.010
Clocking Primitive Attributes
Primitive Instantiated : MMCM
Divide Counter : 3
Mult Counter : 21.625
Clock Phase Shift : None
Clock Wiz O/p Pins
Source
Divider Value
Tspread (ps)
Pk-to-Pk Jitter (ps)
Phase Error (ps)
clk_out1 MMCM CLKOUT0 28.625 OFF 315.002 246.313
clk_out2 OFF OFF OFF OFF OFF
clk_out3 OFF OFF OFF OFF OFF
clk_out4 OFF OFF OFF OFF OFF
clk_out5 OFF OFF OFF OFF OFF
clk_out6 OFF OFF OFF OFF OFF
clk_out7 OFF OFF OFF OFF OFF
OK
Cancel
Divide Counter
Mult Counter
Divider Value

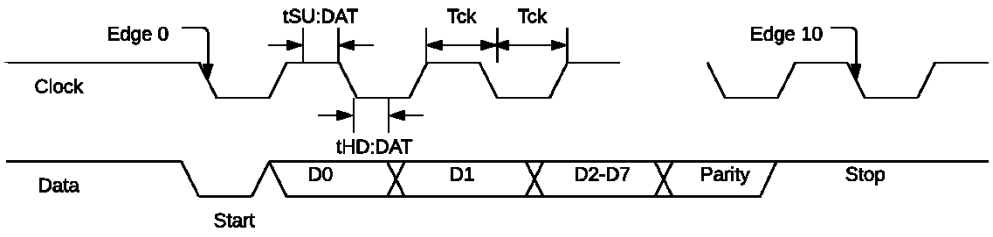

0x32
index
0x6
sub_index
clock
0x32
bitmap

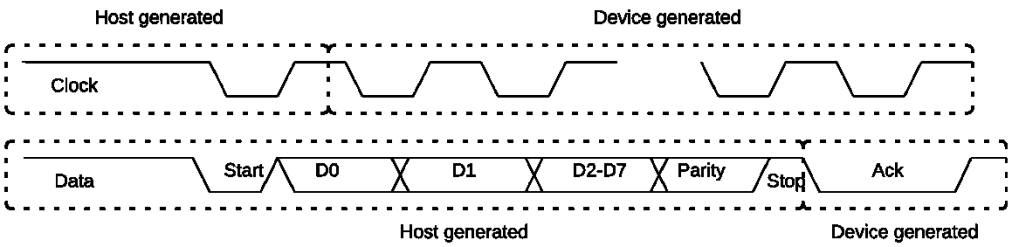


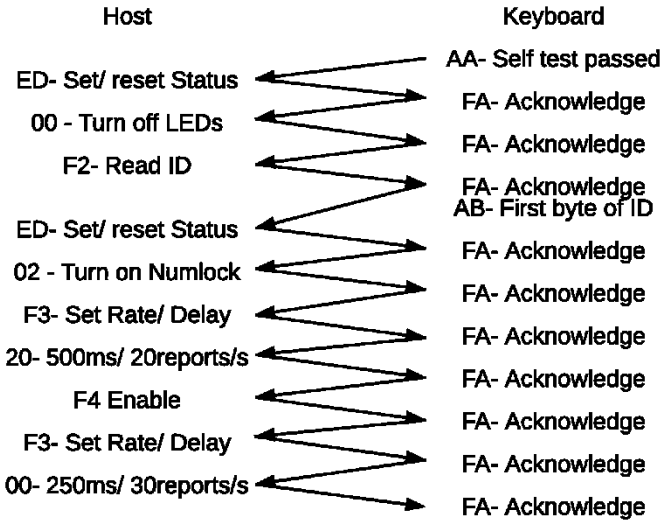

640x480 @ 60Hz
640x480 @ 72Hz
800x600 @ 75Hz
1024x768 @ 70Hz

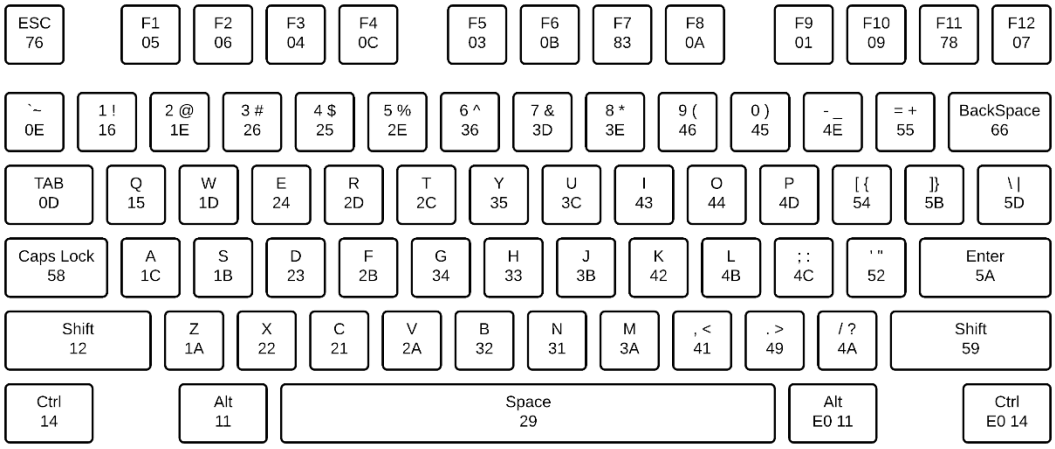
Chapter 10: Bringing It All Together

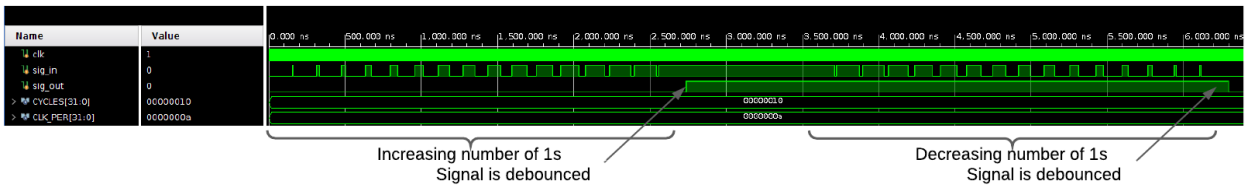





Host generated
Device generated
Clock
Data
Start
D0
D1
D2-D7
Parity
Stop
Ack
Host generated
Device generated


Host
Keyboard
ED- Set/ reset Status
00 - Turn off LEDs
F2- Read ID
ED- Set/ reset Status
02 - Turn on Numlock
F3- Set Rate/ Delay
20- 500ms/ 20reports/s
F4 Enable
F3- Set Rate/ Delay
00- 250ms/ 30reports/s
AA- Self test passed
FA- Acknowledge
FA- Acknowledge
FA- Acknowledge
AB- First byte of ID
FA- Acknowledge
FA- Acknowledge
FA- Acknowledge
FA- Acknowledge
FA- Acknowledge
FA- Acknowledge
FA- Acknowledge


ESC 76
F1 05
F2 06
F3 04
F4 0C
F5 03
F6 0B
F7 83
F8 0A
F9 01
F10 09
F11 78
F12 07
`~ 0E
1 ! 16
2 @ 1E
3 # 26
4 $ 25
5 % 2E
6 ^ 36
7 & 3D
8 * 3E
9 (46
0) 45
- _ 4E
= + 55
BackSpace 66
TAB 0D
Q 15
W 1D
E 24
R 2D
T 2C
Y 35
U 3C
I 43
O 44
P 4D
[{ 54
] } 5B
\ | 5D
Caps Lock 58
A 1C
S 1B
D 23
F 2B
G 34
H 33
J 3B
K 42
L 4B
; : 4C
' " 52
Enter 5A
Shift 12
Z 1A
X 22
C 21
V 2A
B 32
N 31
M 3A
, < 41
. > 49
/ ? 4A
Shift 59
Ctrl 14
Alt 11
Space 29
Alt E0 11
Ctrl E0 14

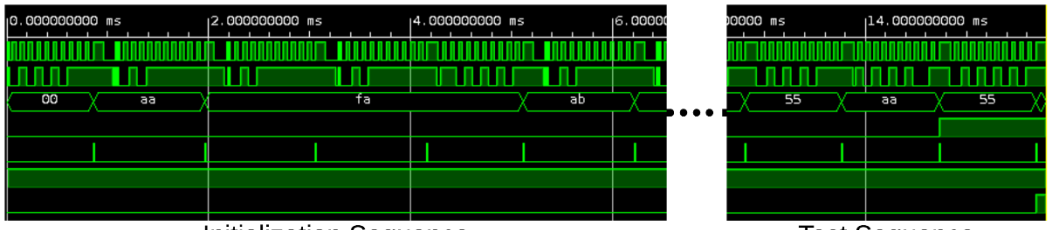

Name
Value
clk
sig_in
sig_out
CYCLES[31:0]
CLK_PER[31:0]
Increasing number of 1s
Signal is debounced
Decreasing number of 1s
Signal is debounced

Fork

```
// 0: send self test passed
repeat (100) @(posedge clk);
send_key(8'hAA, 1'b0);
// Wait for response
rx_key(8'hED);
// 1: send 00
// 2: send f2
// 3: send fA, AB
// 4: send fA
// 5: send fA
// 6: send fA
// 7: send fA
// 8: send fA
r// 9: send fA
repeat (100) @(posedge clk);
send_key(8'hFA, 1'b0);
// Wait for response
rx_key(8'h00);
repeat (100) @(posedge clk);
send_key(8'h55, 1'b0);
repeat (100) @(posedge clk);
send_key(8'hAA, 1'b0);
repeat (100) @(posedge clk);
send_key(8'h55, 1'b1);
repeat (100) @(posedge clk);
send_key(8'hAA, 1'b1);
repeat (100) @(posedge clk);
while (!done) @(posedge clk);
```

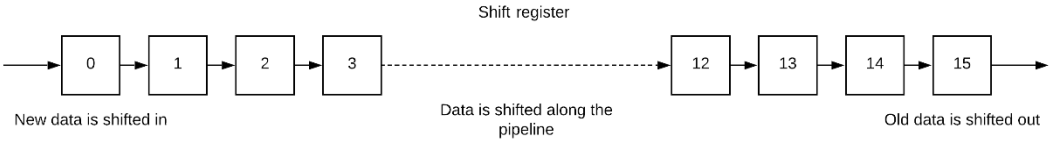
```
// Check keycode received.
while (~done) begin
  while (!rx_valid) @(posedge clk);
  case (valid_count)
    0: begin
      exp_data = 8'h55;
      exp_user = '0;
    end
    1: begin
      exp_data = 8'hAA;
      exp_user = '0;
    end
    2: begin
      exp_data = 8'h55;
      exp_user = '1;
    end
    3: begin
      exp_data = 8'hAA;
      exp_user = '1;
      done = '1;
    end
  endcase // case (valid_count)
  if ((exp_data != rx_data) ||
      (exp_user != rx_user)) begin
    $display("mismatch on output %d", valid_count);
    $stop;
  end else begin
    $display("output matched %d", valid_count);
  end
  valid_count++;
  @(posedge clk);
```

Join



Initialization Sequence

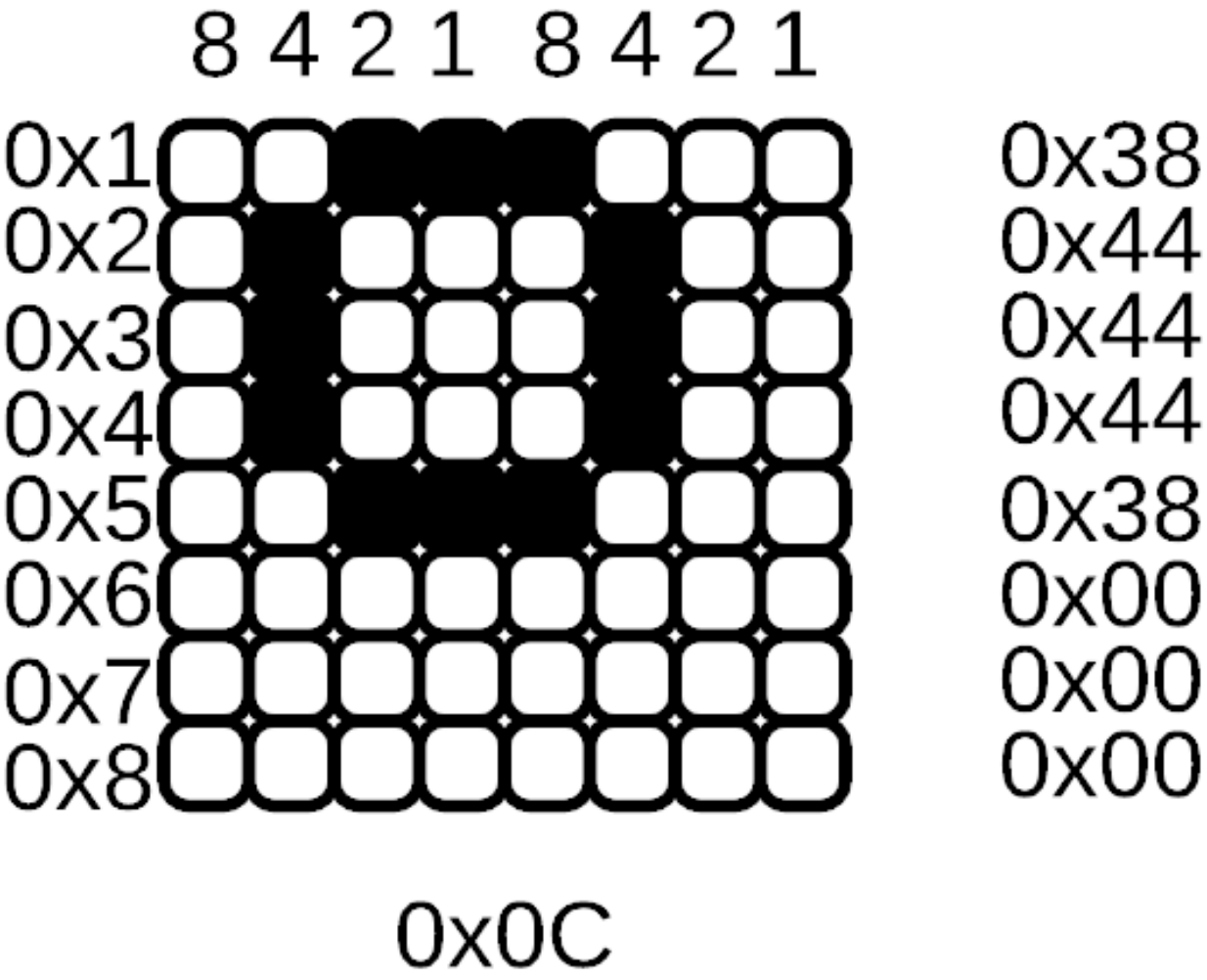
Test Sequence

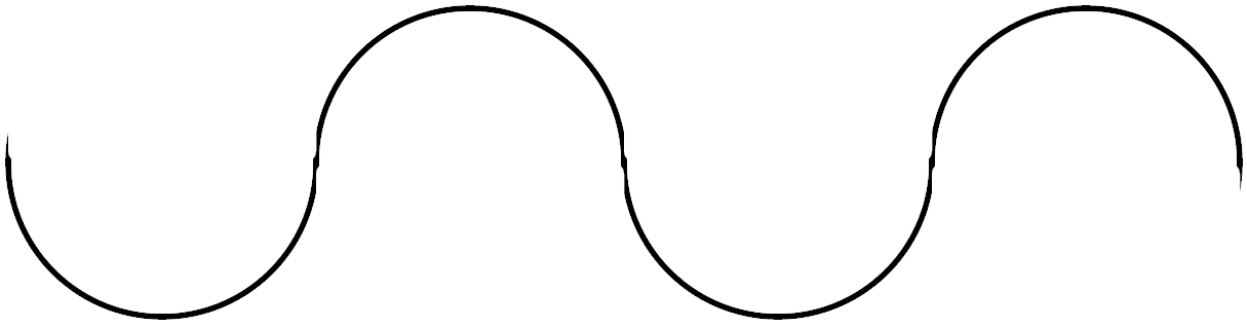


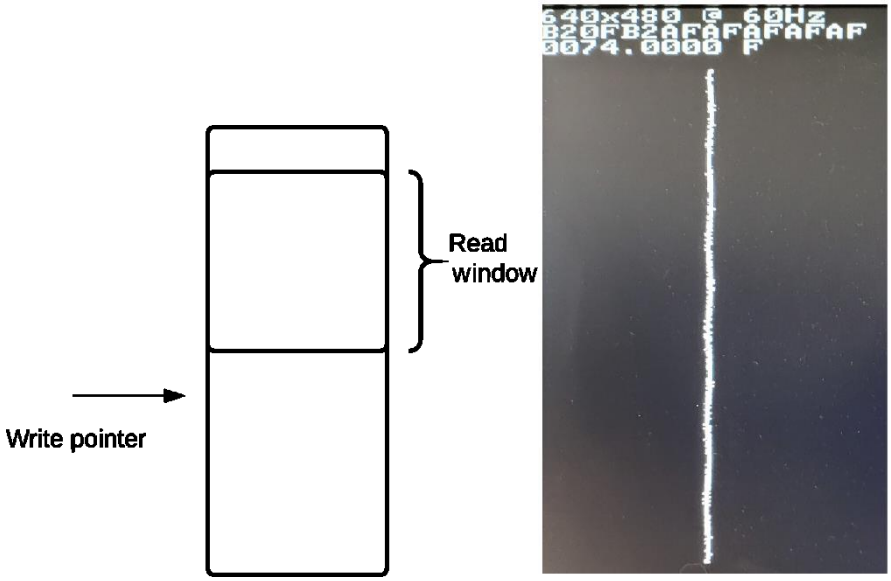
PS/2 Scancodes

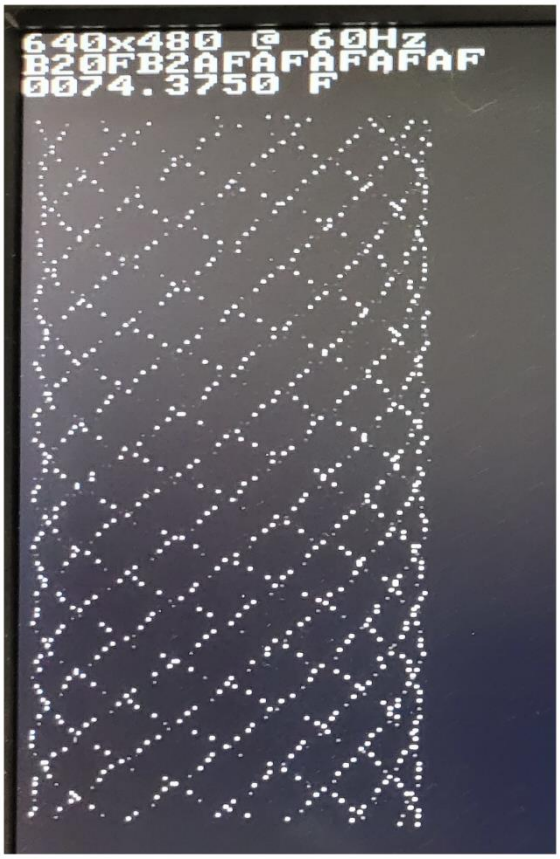
'F' make code

'F' break code

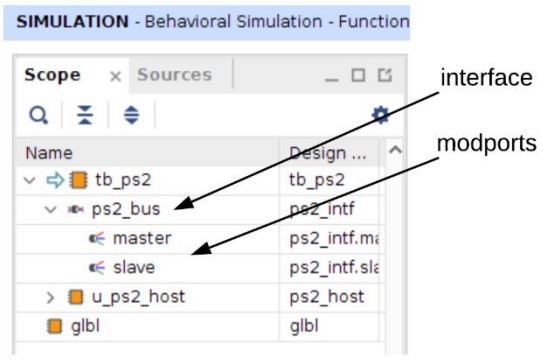


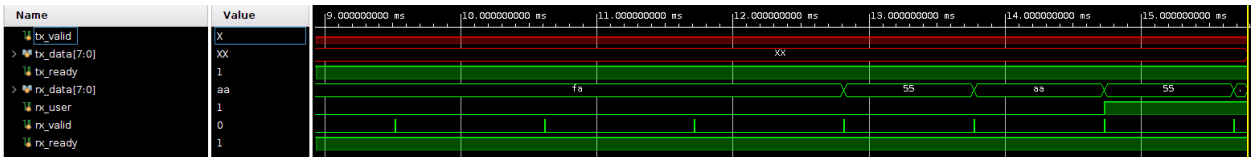


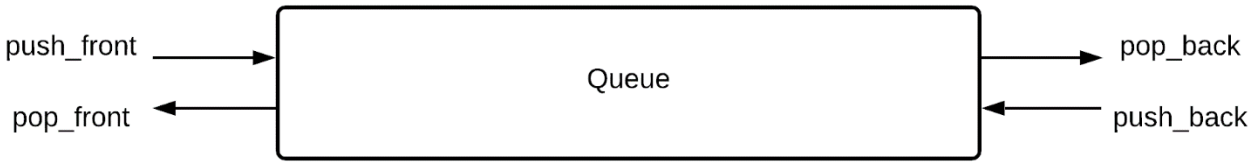

Read
window
Write pointer
640x480 @ 60Hz
B20FB2AFAFAFAFAF
0074.0000 F

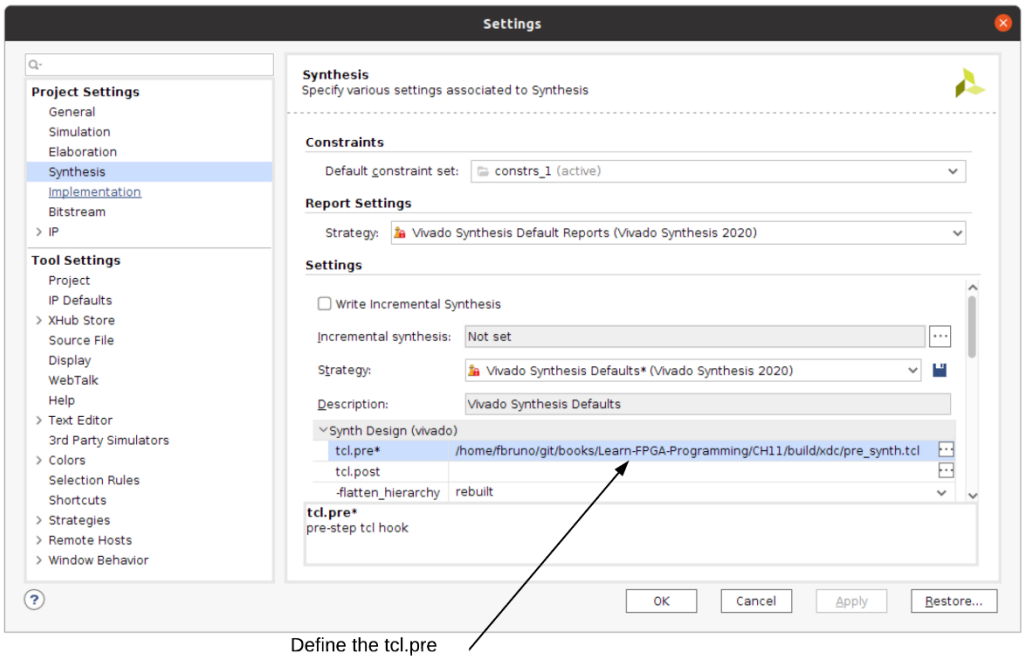

640x480 @ 60Hz
B20FB2AFAFAFAFAF
0074.3750 F

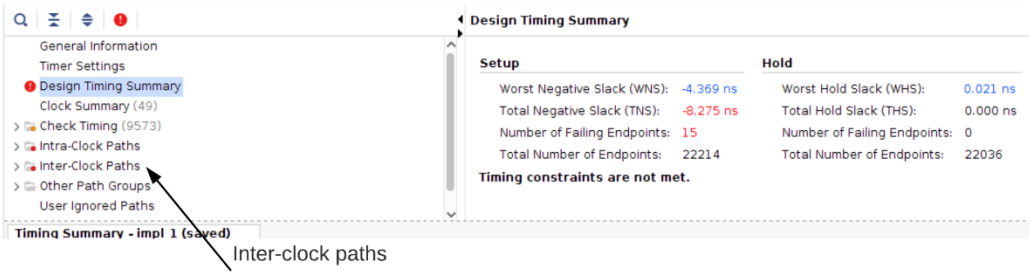
Chapter 11: Advanced Topics

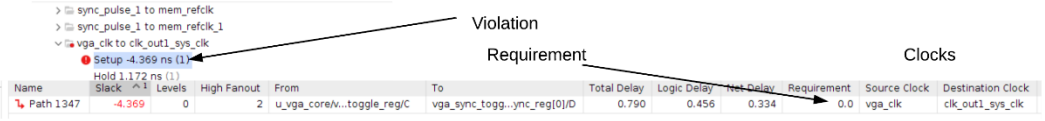


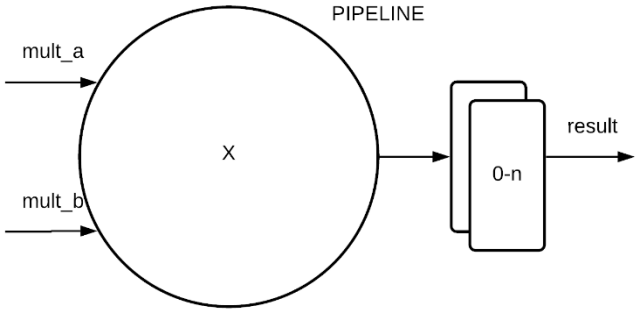


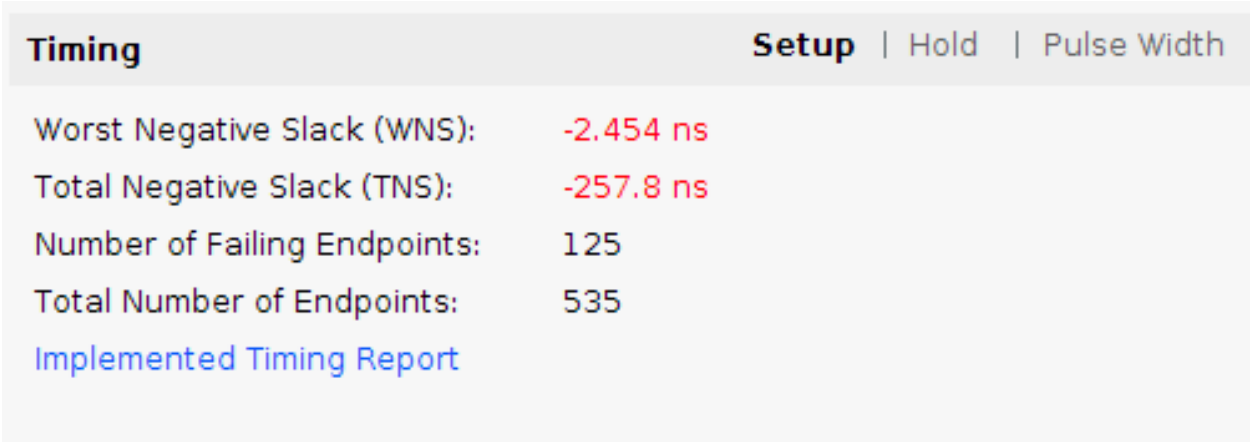


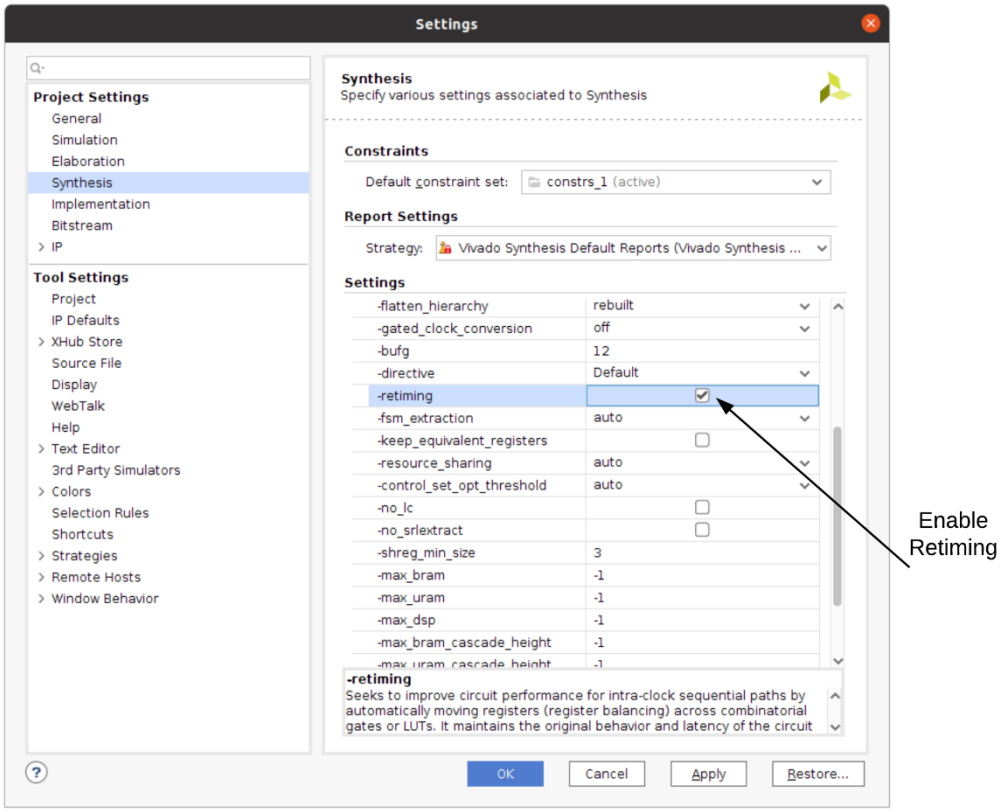


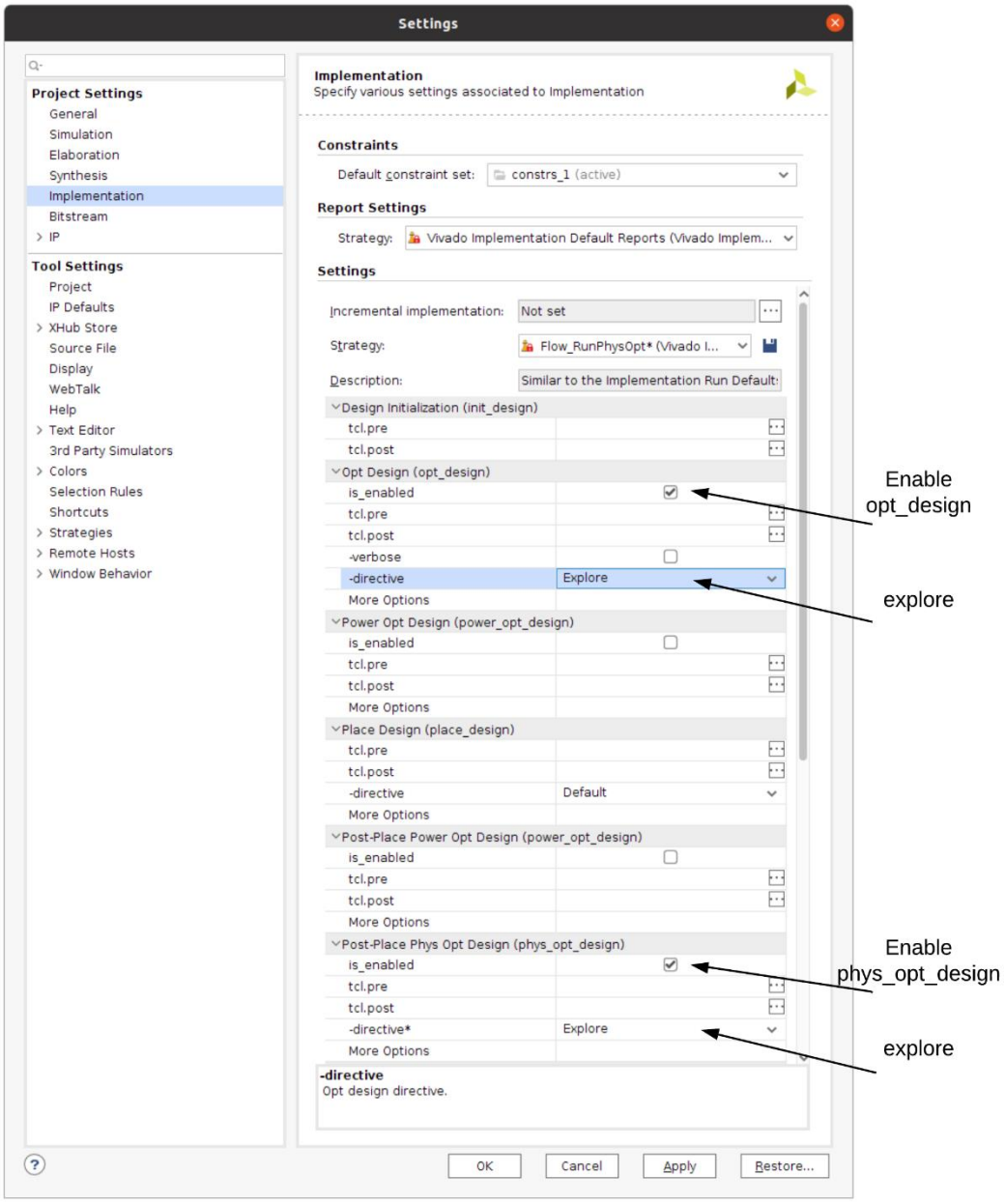

General Information
Timer Settings
Design Timing Summary
Clock Summary (49)
Check Timing (9573)
Intra-Clock Paths
Inter-Clock Paths
Other Path Groups
User Ignored Paths
Timing Summary - impl_1 (saved)
Design Timing Summary
Setup
Worst Negative Slack (WNS): -4.369 ns
Total Negative Slack (TNS): -8.275 ns
Number of Failing Endpoints: 15
Total Number of Endpoints: 22214
Hold
Worst Hold Slack (WHS): 0.021 ns
Total Hold Slack (THS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 22036
Timing constraints are not met.
Inter-clock paths


sync_pulse_1 to mem_refclk
sync_pulse_1 to mem_refclk_1
vga_clk to clk_out1_sys_clk
Setup -4.369 ns (1)
Hold 1.172 ns (1)
Violation
Requirement
Clocks
Name | Slack | Levels | High Fanout | From | To | Total Delay | Logic Delay | Net Delay | Requirement | Source Clock | Destination Clock
Path 1347 | -4.369 | 0 | 2 | u_vga_core/v...toggle_reg/C | vga_sync_togg...ync_reg[0]/D | 0.790 | 0.456 | 0.334 | 0.0 | vga_clk | clk_out1_sys_clk


PIPELINE
mult_a
mult_b
X
0-n
result


Timing
Setup | Hold | Pulse Width
Worst Negative Slack (WNS): -2.454 ns
Total Negative Slack (TNS): -257.8 ns
Number of Failing Endpoints: 125
Total Number of Endpoints: 535
Implemented Timing Report


Settings
Project Settings
General
Simulation
Elaboration
Synthesis
Implementation
Bitstream
IP
Tool Settings
Project
IP Defaults
XHub Store
Source File
Display
WebTalk
Help
Text Editor
3rd Party Simulators
Colors
Selection Rules
Shortcuts
Strategies
Remote Hosts
Window Behavior
Synthesis
Specify various settings associated to Synthesis
Constraints
Default constraint set:
constrs_1 (active)
Report Settings
Strategy:
Vivado Synthesis Default Reports (Vivado Synthesis ...
Settings
-flatten_hierarchy
rebuilt
-gated_clock_conversion
off
-bufg
12
-directive
Default
-retiming
-fsm_extraction
auto
-keep_equivalent_registers
-resource_sharing
auto
-control_set_opt_threshold
auto
-no_lc
-no_srlextract
-shreg_min_size
3
-max_bram
-1
-max_uram
-1
-max_dsp
-1
-max_bram_cascade_height
-1
-retiming
Seeks to improve circuit performance for intra-clock sequential paths by automatically moving registers (register balancing) across combinatorial gates or LUTs. It maintains the original behavior and latency of the circuit
OK
Cancel
Apply
Restore...
Enable
Retiming



Timing

Setup | Hold | Pulse Width

Worst Negative Slack (WNS):	-2.376 ns
Total Negative Slack (TNS):	-250.84 ns
Number of Failing Endpoints:	125
Total Number of Endpoints:	535

Implemented Timing Report

Timing **Setup** | Hold | Pulse Width

Worst Negative Slack (WNS):	-1.139 ns
Total Negative Slack (TNS):	-101.029 ns
Number of Failing Endpoints:	97
Total Number of Endpoints:	631

Implemented Timing Report

Timing **Setup** | Hold | Pulse Width

Worst Negative Slack (WNS):	0.444 ns
Total Negative Slack (TNS):	0 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	617

Implemented Timing Report